LAUTERBACH
DEVELOPMENT TOOLS

Arm Debug and Trace Interface Specification

MANUAL

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History

22-Mar-2024 Fully revised version.

15-Mar-2024 Changed the file name from arm_app_jtag.pdf to app_arm_target_interface.pdf.

Introduction

This application note describes the requirements for seamless compatibility between the debug and trace interface of Arm-based chips and LAUTERBACH tools. It includes specifications for logical functionality, physical connectivity, electrical properties, timing behavior and the design of the printed circuit board (PCB).

The document is intended for:

- Developers looking for guidance on how to connect LAUTERBACH tools to their existing target board.
- Developers of target boards who want to ensure seamless connectivity with LAUTERBACH tools.
- Engineers investigating issues related to an existing interface.

Interface Types, Connectors and LAUTERBACH Probes

When working with LAUTERBACH tools, you always have access to a debug interface, with the option to additionally utilize a trace interface. Most targets feature a debug connector and, optionally, a trace connector. However, there are also targets where both the debug and trace interfaces are provided by a single connector.

There are three types of debug interface standards for the Arm architecture:

- **JTAG**, IEEE 1149.1
- **SWD,** Serial Wire Debug
- **cJTAG**, Compact JTAG, IEEE 1149.7

LAUTERBACH debug probes consistently support all three types. You can select the interface type supported by your target within the TRACE32 GUI. If your target supports multiple debug interface types, you are free to select among them.

There are both parallel and serial trace interfaces available. If your target exports trace data via a PCIe bus, then a PCIe interface is necessary.

The table below enumerates the common target connectors along with the interface types supported by each connector:

Target Connector	Interface Type
ARM-20	debug
MIPI-10	debug
MIPI-20T	debug, 4-bit parallel trace
AUTO-26	debug
Mictor-38	(debug,) parallel trace
MIPI-60	(debug,) parallel trace
Samtec-40	(debug,) serial trace
Samtec-80 (converter to MiniPCIe, PCIe-Slot x1/x4/x8, OCuLink)	PCIe trace

Further details can be found in chapter **"Debug Interface"**, page 16 and **"Trace Interface"**, page 47.

The table before illustrates that in nearly all cases, separate connectors are utilized for debug and trace interfaces. The lone exception is the MIPI-20T connector, which supports both interfaces concurrently.

The trace connectors Mictor-38, MIPI-60, and Samtec-40 can also be used for the debug interface. This not only conserves connectors but also saves space on the target hardware. However, it's important to note that when connecting a Debug Cable or HS Whisker to the target, a converter is necessary, such as ARM-20 to Mictor-38.

To facilitate the use of a common connector, Lauterbach trace probes offer the flexibility of connecting either the Debug Cable or HS Whisker. For details regarding which connector is provided by individual trace probes, please consult the subsequent table. The photo depicts the ARM-20 connector supplied by the trace probes AutoFocus II Preprocessor and the HSSTP Preprocessor.

The subsequent table outlines the probe connectors provided by each LAUTERBACH probe, along with usage hints and important notes. LAUTERBACH provides converters for compatibility if the probe connector does not align with your target connector:

Probe	Probe Connector	Usage Hints	Note
IDC20A Debug Cable	**ARM-20**	robust debug connector	
HS Whisker (µTrace or CombiProbe)	**MIPI-20T**	small debug connector with 4-bit low bandwidth parallel trace port	trace bandwidth is sufficient for most Cortex-M cores or system trace such as ITM/STM
	MIPI-10	smallest debug connector	

Probe	Probe Connector	Usage Hints	Note
AUTO26 Debug Cable	AUTO-26	only use this debug connector if concurrent use is required	facilitates concurrent utilization of the debug interface by a calibration tool (automotive sector)
	MIPI-20T	small debug connector	unlike HS Whisker, the trace pins cannot be used the primary tool used with this connector is the HS Whisker
	MIPI-10	small debug connector	the primary tool used with this connector is the HS Whisker
AutoFocus II Preprocessor	Mictor-38	robust parallel trace connector single Mictor-38 for up to 16 bit two Mictor-38 for up to 32 bit	Mictor-38 connector is the preferred connector for parallel trace ports enables an ARM-20 connection when the debug interface is also utilized through the Mictor-38 connector
AutoFocus II MIPI Preprocessor	MIPI-60	parallel trace connector for up to 32 bit	typically used with Texas Instruments evaluation boards enables a MIPI34 connection when the debug interface is also utilized through the MIPI-60 connector
HSSTP Preprocessor	Samtec-40	serial trace connector, up to 4 lanes	outdated probe, should only be utilized if PowerTrace II/III is accessible and the lower bandwidth meets the requirements enables an ARM-20 connection when the debug interface is also utilized through the Samtec-40 connector

Probe	Probe Connector	Usage Hints	Note
PowerTrace Serial HSSTP	**Samtec-40**	serial trace connector, up to 6 lanes (8 lanes with Samtec-80)	standard solution enables an MIPI34 connection when the debug interface is also utilized through the Samtec-40 connector
Aurora 2 Preprocessor connected to PowerTrace Serial	**Samtec-40**	serial trace connector, up to 4 lanes at higher speed	
PowerTrace Serial PCIe	**Samtec-80**	serial trace connector, up to 8 lanes	typically used with converter for PCIe slots or OKuLink connector on the target

LAUTERBACH Probe Description

This chapter provides an introduction to the individual Lauterbach probes. It includes a photograph depicting the probe within a fully operational TRACE32 tool configuration. Additionally, details regarding the probe connector and the supported interface type are provided.

IDC20A Debug Cable

Picture: ICD20A Debug Cable on a PowerDebug base module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug modules along with their respective delivery periods.

Connector: **ARM-20**

Interface type: debug

Dimension: A drawing illustrating the dimensions of the IDC20A Debug Cable is available at **www2.lauterbach.com/size/si_3000.pdf**.

HS Whisker

Picture: HS Whisker on CombiProbe 2 connected to a PowerDebug base module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug modules along with their respective delivery periods.

Connector: **MIPI-10, MIPI-20T,** both via the included matching cable

Interface type: debug, optional 4 bit parallel trace (only with MIPI-20T)

AUTO26 Debug Cable

Picture: AUTO26 Debug Cable connected to a PowerDebug base module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug modules along with their respective delivery periods.

Connector: **MIPI-10, MIPI-20T, AUTO26,** all via the included matching cable

Interface type: debug

AutoFocus II Preprocessor

Picture: AutoFocus II Preprocessor connected to PowerTrace module and IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **Mictor-38** via the included Mictor flex extension

Interface type: (debug), parallel trace

Dimension: A drawing illustrating the dimensions of the Mictor-38 flex extension is available at **www2.lauterbach.com/size/si_1370.pdf**.

AutoFocus II MIPI Preprocessor

Picture: AutoFocus II MIPI Preprocessor connected to PowerTrace module and IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **MIPI-60** via the included flex extension for Samtec-60

Interface type: (debug,) parallel trace

Dimension: A drawing illustrating the dimensions of the Samtec-60 flex extension is available at **www2.lauterbach.com/size/si_1228.pdf**.

HSSTP Preprocessor

Picture: HSSTP Preprocessor connected to PowerTrace module and IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **Samtec-40** via included flex extension for Samtec-40

Interface type: (debug,) serial trace

Dimension: A drawing illustrating the dimensions of the Samtec-40 flex extension is available at **www2.lauterbach.com/size/si_1232.pdf**.

PowerTrace Serial HSSTP

Picture: PowerTrace Serial and IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **Samtec-40** via included flex extension for Samtec-40

Interface type: (debug,) serial trace

Aurora 2 Preprocessor

Picture: Aurora 2 Preprocessor connected to a PowerTrace Serial, IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **Samtec-40** via included flex extension for Samtec-40

Interface type: serial trace

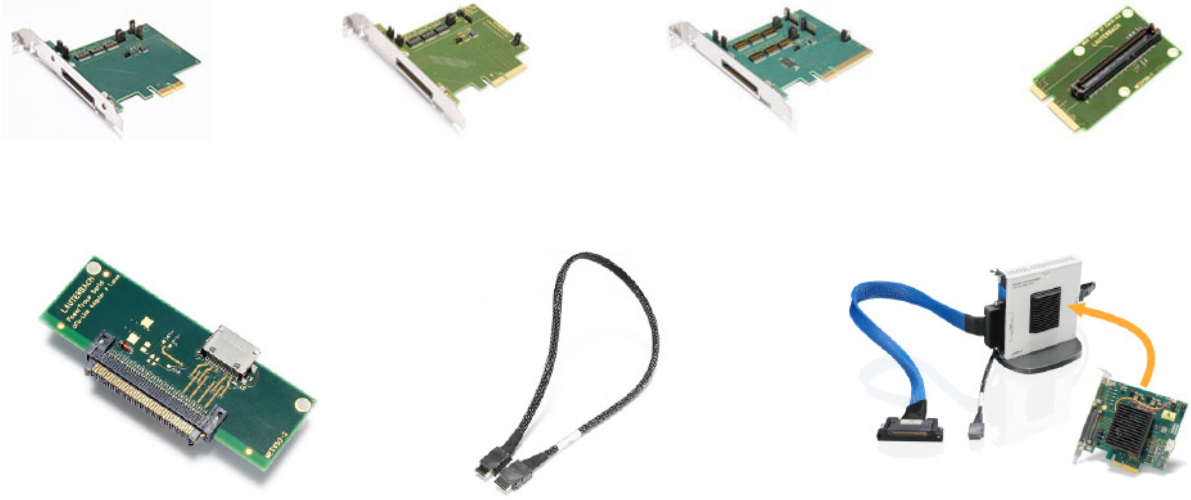
Picture: PowerTrace Serial and IDC20A Debug Cable connected to PowerDebug module.

The chapter **"TRACE32 Product Story"** in TRACE32 Terminology, page 9 (trace32_terms.pdf) outlines the various versions of the PowerDebug and PowerTrace modules along with their respective delivery periods.

Connector: **Samtec-80** via included flex extension for Samtec-80

Interface type: PCIe trace

Converters



Picture: Converters from Samtec-80 to PCIe-Slot x1 (LA-3527), PCIe-Slot x4 (LA-3524), PCIe-Slot x8 (LA-3525), MiniPCIe (LA-3526), OCuLink (LA-3590+LA-1990), PCIe-Slot x4 or OCuLink with PCIe Gen 4 Preprocessor (LA-3529).

Connector: PCIe-Slot x1/x4/x8, MiniPCIe, OCuLink (description see industry standard)

Interface type: PCIe trace

Debug Interface

Introduction

Three Debug Interface Standards

Three standards can be used for the debug interface:

- **JTAG**, IEEE 1149.1
- **SWD**, Serial Wire Debug, an Arm standard
- **cJTAG**, Compact JTAG, IEEE 1149.7

cJTAG is seldom utilized and not advisable if alternatives like JTAG or SWD are available, as it operates significantly slower.

All debug connectors and all our debug probes support JTAG, SWD and cJTAG. The JTAG signals TCK and TMS are reused for SWD and cJTAG. The following interface description therefore covers all three interfaces at once.

Required Signals

Depending on the standard used, you will need in addition to VREF-DEBUG and GND:

- JTAG: TCK, TMS, TDI, TDO, (TRST-)
- SWD: SWCLK, SWDIO, (SWO)
- cJTAG: TCKC, TMSC

It is recommended that you also use RESET-.

On-Chip Trace

The debug interface is also sufficient for on-chip trace, as the trace recording is stored in real time in a memory on the chip and the trace data is read out more slowly via the debug interface after recording.

Serial Wire Viewer (SWV) / Serial Wire Output (SWO)

Further Arm's one-pin-trace port called Serial Wire Viewer (SWV) / Serial Wire Output (SWO) is described together with our debug interface here, because the JTAG signal TDO is re-used for that purpose. So, pinout and electrical specification is the same as for JTAG/TDO. SWV/SWO is supported by all newer debug probes and newer base modules, i.e. HS Whisker on µTrace or CombiProbe, AUTO26 Debug Cable version V2 or newer (delivered from 2021), IDC20A Debug Cable version V5 or newer (delivered from 2018) and base modules such as PowerDebug PRO/E40/X50 or newer models. SWV/SWO is typically found on small Cortex-M-based microcontrollers with a small number of pins.

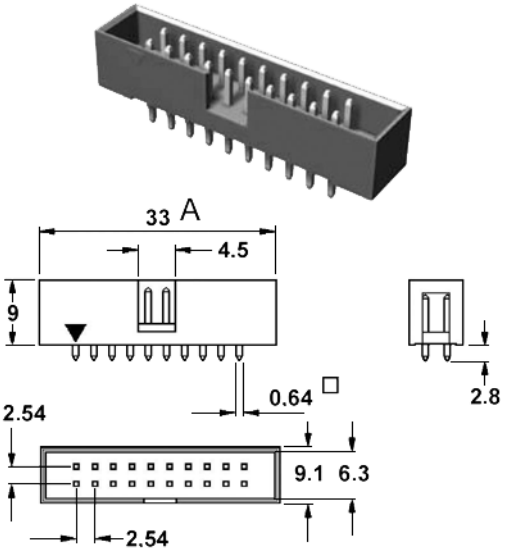
ARM-20

Pinout:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	VSUPPLY (not used)
TRST-	3	4	GND
TDI	5	6	GND
TMS|TMSC|SWDIO	7	8	GND
TCK|TCKC|SWCLK	9	10	GND
RTCK	11	12	GND
TDO|-|SWO	13	14	GND
RESET-	15	16	GND
DBGRQ	17	18	GND
DBGACK	19	20	GND

For a comprehensive description of all signals displayed in the pinouts, refer to the **“Debug Signals”**, page 22.

Target Connector:



The target board requires a standard 20 pin double row male connector, pin to pin spacing 2.54mm/0.100" x 2.54mm/0.100" and 0.025" square post width. A shrouded connector with center polarization is recommended.

Placement:

Please refer to the general recommendations outlined in the chapter **“General Recommendations for Debug Connector Placement”**, page 44.

We recommend placing the even numbered pins on the edge of the board (probe flex cable won't get twisted).

Examples with housing: Samtec HTST-110-01-L-D (through-hole), Samtec HTST-110-01-L-DV (surface mount)

Examples without housing: Samtec TSW-110-23-L-D, Berg: 67996-120H

MIPI-20T

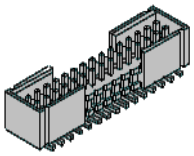
MIPI-20T is equivalent to Arm's “CoreSight 20”, except that MIPI-20T has pins 11 and 13 connected to GND (instead of N/C).

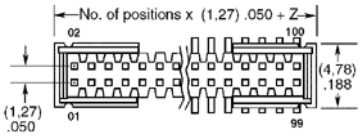
Pinout:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
GND	3	4	TCK|TCKC|SWCLK
GND	5	6	TDO|-|SWO
GND (KEY)	-	8	TDI
GND	9	10	RESET-
GND	11	12	TRACECLK
GND	13	14	TRACEDATA[0]
GND	15	16	TRACEDATA[1]
GND	17	18	TRACEDATA[2]
GND	19	20	TRACEDATA[3]

For a comprehensive description of all signals displayed in the pinouts, refer to the **“Debug Signals”**, page 22.

Target Connector:





The target board requires a 20 pin double row male connector with 1.27mm/0.050" x 1.27mm/0.050" pin to pin spacing and 0.016" square post width. A shrouded connector with center polarization is recommended. Pin 7 is a key pin that prevents mating in the wrong orientation. Therefore, pin 7 must be removed on the target side.

Placement:

Please refer to the general recommendations outlined in the chapter **"General Recommendations for Debug Connector Placement"**, page 44.

We recommend placing the odd numbered pins on the edge of the board (probe flex cable won't get twisted).

Example with housing: Samtec FTSH-110-01-L-DV-K (surface mount)

MIPI-10

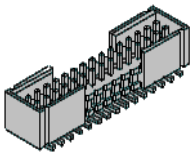
MIPI-10 is equivalent to Arm's "CoreSight 10".

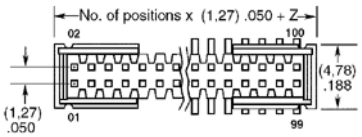
Pinout:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
GND	3	4	TCK|TCKC|SWCLK
GND	5	6	TDO|-|SWO
GND (KEY)	-	8	TDI
GND	9	10	RESET-

For a comprehensive description of all signals displayed in the pinouts, refer to the **"Debug Signals"**, page 22.

Target Connector:





The target board requires a 10 pin double row male connector with 1.27mm/0.050" x 1.27mm/0.050" pin to pin spacing and 0.016" square post width. A shrouded connector with center polarization is recommended. Pin 7 is a key pin that prevents mating in the wrong orientation. Therefore, pin 7 must be removed on the target side.

Placement:

Please refer to the general recommendations outlined in the chapter **"General Recommendations for Debug Connector Placement"**, page 44.

We recommend placing the odd numbered pins on the edge of the board (probe flex cable won't get twisted).

Example with housing: Samtec FTSH-105-01-L-DV-K (surface mount)

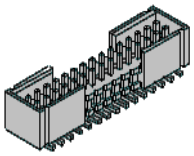
AUTO-26

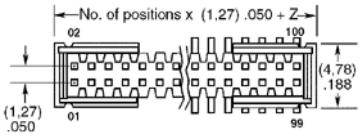
Pinout:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
GND	3	4	TCK|TCKC|SWCLK
GND	5	6	TDO|-|SWO
GND (KEY)	-	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	TRST- PULLDOWN
GND	15	16	TRST-
GND	17	18	DBGRQ (EMU0)
GND	19	20	DBGACK (EMU1)
GND	21	22	BREQ-
GND	23	24	BGRNT-
GND	25	26	EXTIO

For a comprehensive description of all signals displayed in the pinouts, refer to the **"Debug Signals"**, page 22.

Target Connector:





The target board requires a 26 pin double row male connector with 1.27mm/0.050" x 1.27mm/0.050" pin to pin spacing and 0.016" square post width. A shrouded connector with center polarization is recommended. Pin 7 is a key pin that prevents mating in the wrong orientation. Therefore, pin 7 must be removed on the target side.

Placement:

Please refer to the general recommendations outlined in the chapter **"General Recommendations for Debug Connector Placement"**, page 44.

We recommend placing the odd numbered pins on the edge of the board (probe flex cable won't get twisted).

Example with housing: Samtec FTSH-113-01-L-DV-K (surface mount)

MIPI-20D, MIPI-34

These two debug probe connectors are outdated and are not described in this manual. Previously, for the CombiProbe, there was a MIPI34 Whisker and corresponding converters available.

- The AutoFocus II MIPI Preprocessor still features a MIPI-34 connector in case the MIPI-60 connector on the target is also used for the debug interface.
- The PowerTrace Serial still features a MIPI-34 connector in case the Samtec-40 connector on the target is utilized for the debug interface.

Both tools come with a converter for ARM20/IDC20A to MIPI-34 (see **converter for ARM-20**). In the event that you are using an HS Whisker, there is a MIPI-20T to MIPI-34 converter available (**LA-2774**).

Debug Signals

The MIPI-20T trace signals are described in chapter **"Trace Interface"**, page 47. VREF-DEBUG is used as the trace voltage reference on this connector (same voltage reference as debug).

If you do not need or wish to utilize any of the signals outlined below, we advise against connecting them. Each signal is terminated on the Lauterbach probe side. Please refrain from using any signal for alternative purposes, as it is connected to drivers/receivers on the Lauterbach probe side. Only VSUPPLY is not connected to the Lauterbach probes.

Signal / Direction	Description	Compliance	Recommendation
BGRNT- to debugger	The “Bus Grant” (low active) signal grants the interface usage when employed alongside another tool, such as a calibration tool.	Exclusive to AUTO-26. Only necessary when sharing the debug interface, such as with a calibration tool.	Only necessary when sharing the debug interface, such as with a calibration tool. Otherwise, do not connect.
BREQ- from debugger	“Bus Request” (low active) requests the interface for use when it is used together with another tool such as a calibration tool.	Only with AUTO-26. Only necessary when sharing the debug interface, such as with a calibration tool.	Only necessary when sharing the debug interface, such as with a calibration tool. Connect to GND otherwise.
DBGACK to debugger	“Debug Acknowledge“ (active high) serves as an input for the debugger to detect the processor's halt status. However, this signal is largely absent in modern chips. Synchronous halting is typically achieved through an internal cross-trigger matrix (CTI/CTM) within the chip. If accessible, it can be utilized for rapid triggering, such as synchronously halting all chips within a multichip system.	Is typically unnecessary.	Do not connect.

Signal / Direction	Description	Compliance	Recommendation
DBGRQ from debugger	The “Debug Request” (active-high) signal serves as an output from the debugger, aimed at transitioning the processor into debug mode, thereby stopping program execution. While the debugger offers alternative methods to stop program execution, initiating a '“Debug Request” remains the fastest approach. However, this signal is largely absent in modern chips. Synchronous halting is typically achieved through an internal cross-trigger matrix (CTI/CTM) within the chip.	Not required anymore.	Do not connect. If this signal is provided by the processor you should pull it down on the target side to keep the signal in the inactive state.
EXTIO from/to debugger	“External IO”. This is a software configurable input/output. Reserved for future use.	Exclusive to AUTO-26. Not required.	Do not connect.
GND	”Ground”.	Mandatory.	Connect all GND pins to minimize noise interference.
GND (KEY)	This pin serves as a key to prevent incorrect connection of the debug probe to the target hardware. It should be physically cut off on the target connector and is already blocked on the LAUTERBACH probe upon delivery.	Recommen-ded.	No electrical function. Protection against incorrect connection.

Signal / Direction	Description	Compliance	Recommendation
RESET- from/to debugger	The “System Reset" signal (low active) is used to reset the target system. Additionally, the debugger uses this signal to determine whether the processor is held in reset. This functionality is not mandatory. If the current reset status is not signaled via this line, this pin should be continuously high (= no reset).The debugger controls this pin as an open-drain output (in contrast to other outputs, which are push-pull). A 47 kΩ pull-up resistor is located inside the debug probe. See important notes in chapter **“Reset Considerations”**, page 45.	Optional.	Recommended. It may be necessary to include a pull-up resistor (1 kΩ - 47 kΩ) on the target side to prevent unintended resets when the debugger is disconnected. Additionally, it might be advisable to strengthen the weak 47 kΩ pull-up in the debug probe.
RTCK to debugger	“Return Test Clock" was used to synchronize the JTAG signals with the internal clocks of some older ARM7, ARM9 and ARM11 cores. This is not required for CoreSight and/or Cortex cores.	Not required anymore.	Do not connect. Especially avoid connecting it to TCK, as this creates a stub on the TCK line, a common source of signal issues we often encounter on customer boards.
SWCLK from debugger	“Serial Wire Clock” is the SWD clock signal from debugger to processor.	Required for SWD.	You should place a pull-down resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
SWDIO from/to debugger	“Serial Wire Data I/O” is the SWD data signal from debugger to processor and vice versa.	Required for SWD.	You can place a 47 Ω series resistor near the processor for the serial termination, if the chip's output driver is not impedance matched. You can place a pull-up resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.

Signal / Direction	Description	Compliance	Recommendation
SWO to debugger	The “Serial Wire Output” is an optional single-pin asynchronous trace port with very low bandwidth. It can be utilized alongside the SWD interface, provided that the chip supports it.	Required only if SWO is available and intended for use.	You can place a 47 Ω series resistor near the processor for the serial termination, if the chip's output driver is not impedance matched. You can place a pull-up (or pull-down) resistor (1 kΩ - 47 kΩ) on this line.
TCK from debugger	“Test Clock” is the JTAG clock signal from debugger to processor.	Required for JTAG.	You should place a pull-down resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
TCKC from debugger	“Test Clock Compact” is the cJTAG clock signal from debugger to processor.	Required for cJTAG.	You should place a pull-down resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
TDI from debugger	“Test Data In” is the JTAG data signal from debugger to processor.	Required for JTAG.	You can place a pull-up (or pull-down) resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
TDO to debugger	“Test Data Out” is the JTAG data signal from processor to debugger.	Required for JTAG.	You can place a 47 Ω series resistor near the processor for the serial termination, if the chip's output driver is not impedance matched. You can place a pull-up (or pull-down) resistor (1 kΩ - 47 kΩ) on this line.
TMS from debugger	“Test Mode Select” is the JTAG control signal for the TAP controller.	Required for JTAG.	You can place a pull-up resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.

Signal / Direction	Description	Compliance	Recommendation
TMSC from/to debugger	“Test Mode Select Compact” is the cJTAG data signal from debugger to processor and vice versa.	Required for cJTAG	You can place a 47 Ω series resistor near the processor for the serial termination, if the chip's output driver is not impedance matched. You can place a pull-up resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
TRST- from debugger	”Test Reset” (low active) is used for an asynchronous reset of the JTAG Test Access Port (TAP). It resets the TAP state machine. The debugger controls this signal using a push-pull driver. From the debugger's perspective, this signal is optional, as it can alternatively reset the TAP using a specific JTAG sequence. A pull-down on target side is not JTAG compliant, but ensures that the on-chip debug logic is inactive if the debugger is not connected. See important notes in chapter **“Reset Considerations”**, page 45.	Only with JTAG. Optional if TRST- has a pull-up on target side. Required if TRST- has a pull-down on target side.	Recommended to connect if the chip provides this signal; otherwise, leave it unconnected. You should place a pull-up (or pull-down) resistor (1 kΩ - 47 kΩ) on this signal in order to give it a defined state when the signal is not driven by the debugger.

Signal / Direction	Description	Compliance	Recommendation
TRST- PULL DOWN from debugger	“Test Reset” (low active) is used for an asynchronous reset of the JTAG Test Access Port (TAP). It resets the TAP state machine. This signal shall be used instead of TRST- if there is a pull-down on this line on the target side, although the function is identical. The debugger controls it via a push-pull driver. From the debugger’s point of view, it is optional, as it also resets the TAP using a specific JTAG sequence. A pull-down on target side is not JTAG compliant, but ensures that the on-chip debug logic is inactive if the debugger is not connected. See important notes in chapter **“Reset Considerations”**, page 45.	Only with JTAG. Optional if TRST- has a pull-up on target side. Required if TRST- has a pull-down on target side.	Recommended if the chip provides this signal, otherwise leave unconnected. You should place a pull-up (or pull-down) resistor (1 kΩ - 47 kΩ) on this line in order to give it a defined state when the line is not driven by the debugger.
VREF- DEBUG to debugger	“Voltage Reference Debug” is the target reference voltage for the debug signals. This line indicates the presence of target power. It serves to establish the logic level reference (VREF/2) for the debugger input comparators and automatically adjusts the voltage levels of the debugger output drivers.	Required.	It should be directly connected to the power supply of the processor's IO pins. While a series resistor is permissible, it is not advisable. The signal must be robust enough to overpower an approximately 10 kΩ pull-down resistor in the debug probe.
VSUPPLY to debugger	Other debuggers utilize “Voltage Supply” to source their supply current. However, LAUTERBACH debug probes have their own dedicated power supply and do not rely on this feature. As such, this line is not utilized.	Not used by LAUTER-BACH debug probes.	Do not connect. For powering non-LAUTERBACH debug tools, you may connect this signal directly to a 5 V or 3.3 V power supply, without the use of a series resistor.

DC Electrical Characteristics

The following table describes the DC electrical characteristics of the debug probes. The current values are measured in the positive direction from the debug probe to the target system. The characteristics apply to the full operating range of the target system. The following values are for reference only and are not guaranteed by LAUTERBACH.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Vvref	VREF-DEBUG operating voltage	IDC20A	0.38		5.25	V
		HS Whisker	1.8		5.25	V
		AUTO26	1.2		5.25	V
Vvref_pwrdwn	VREF-DEBUG power down indication	IDC20A	-0.3	0.27	0.35	V
		HS Whisker	-0.3	0.8	0.9	V
		AUTO26	-0.3	1.65	1.75	V
Ivref	VREF-DEBUG current	Vvref = 5.25V IDC20A HS Whisker AUTO26		 -0.05 -0.525 -0.525	 -0.1 -0.53 -0.53	mA
Vil	Low-level input voltage	IDC20A Vvref = 1.5V Vvtef = 1.8V Vvtef = 2.5V Vvref = 3.3V Vvref = 5.0V	-0.3	 0.6 0.75 1.1 1.5 2.3	0.3 * Vvref	V
		HS Whisker Vvref = 1.2V Vvtef = 1.8V Vvref = 2.5V Vvref = 3.3V Vvref = 5.0V	-0.3		 0.24 0.63 0.7 0.8 1.5	V
		AUTO26 Vvref = 1.8V Vvref = 2.5V Vvref = 3.3V Vvref = 5.0V	-0.3		 0.63 0.7 0.8 1.5	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Vih	High-level input voltage	IDC20A Vvref = 1.5V Vvref = 1.8V Vvref = 2.5V Vvref = 3.3V Vvref = 5.0V	0.7 * Vvref	 0.9 1.0 1.4 1.8 2.6	5.25	V
		HS Whisker Vvref = 1.2V Vvref = 1.8V Vvref = 2.5V Vvref = 3.3V Vvref = 5.0V	 0.96 1.17 1.7 2.0 3.5		5.25	V
		AUTO26 Vvref = 1.8V Vvref = 2.5V Vvref = 3.3V Vvref = 5.0V	 1.17 1.7 2.0 3.5		5.25	V
Vol	Low-level output voltage		0	(1)	0.3 * Vvref	V
Voh	High-level output voltage		0.7* Vvref	(1)	Vvref	V
Iil	Low-level input current				0.2	mA
Iih	High-level input current				-0.2	mA
Iol	Low-level output current	Vvref < 1.5V Vvref >= 1.5V Vol < 0.3*Vvref			-2 -6	mA
Ioh	High-level output current	Vvref < 1.5V Vvref >= 1.5V Voh > 0.7*Vvref			2 6	mA

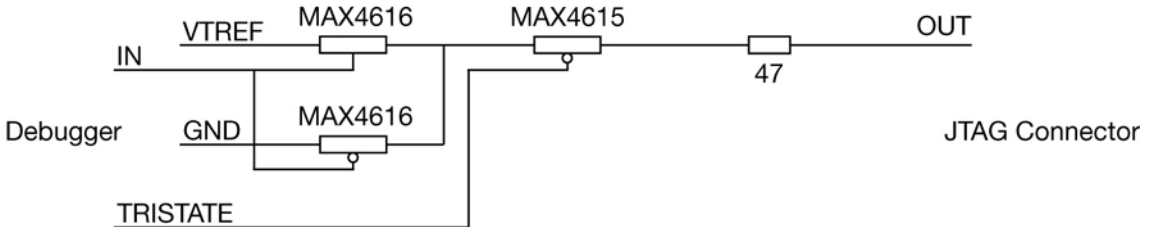
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Rreset	RESET- pin pullup (2)	IDC20A		47		kΩ
		HS Whisker		220		kΩ
		AUTO26		10		kΩ

(1) Typical value dominated by 47 Ω series resistor between driver and debug cable. For example, at Iol = -6 mA or Ioh = 6 mA, expect a 0.3 V drop relative to GND or Vvref potential.
(2) An additional pull-up on target side might be required if target operation without attached debugger is desired.

Debug Probe Driver/Receiver (IDC20A)

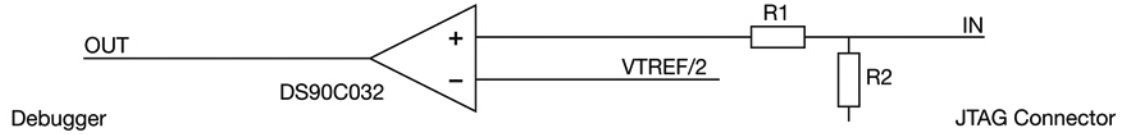
This chapter describes the actual driver/receiver circuit inside the IDC20A Debug Cable. For additional information, refer to the MAX4616, MAX4615 and DS90C032 data sheets.

Output Circuitry



The output signals TCK, TMS, TDI, TRST-, DBGRQ are controlled by analog switches that switch the signal level to VREF-DEBUG (supplied by the debugger), GND, respectively. Another analog switch is used to tristate this output signal. A 47 Ω resistor is used for current limiting and serial termination. RESET- has a 47 kΩ pull-up instead of the analog switch to VREF-DEBUG (see **Input Circuitry**).

Input Circuitry



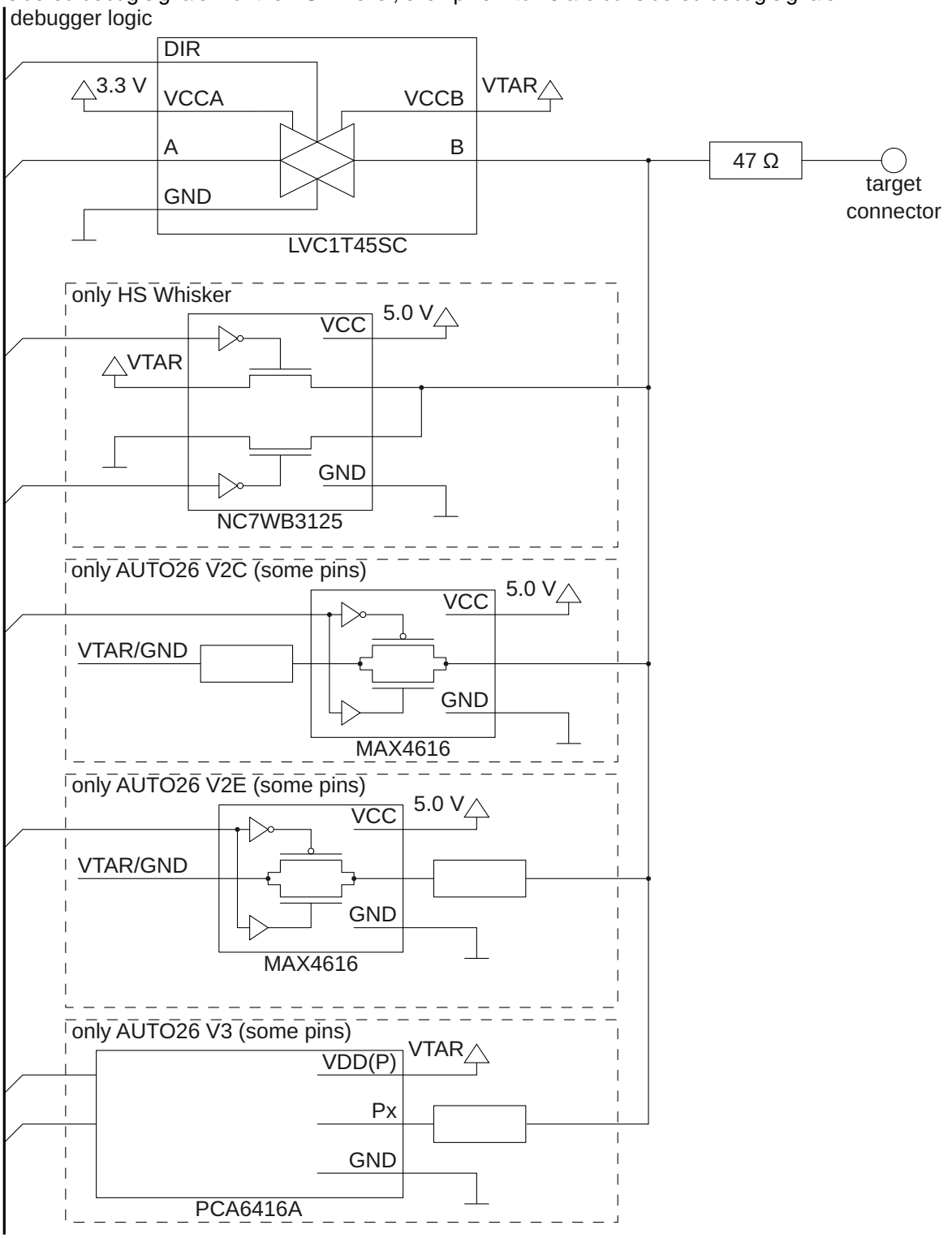
The input signals TDO, RTCK, DBGACK, RESET- are compared to VREF-DEBUG/2.

Signal	R1	R2
RTCK	0 Ω	47 kΩ pull-down, parallel to R2: termination 220 Ω, 220 pF
TDO	0 Ω	100 kΩ pull-down

Signal	R1	R2
DBGACK	1 kΩ	47 kΩ pull-down
RESET-	0 Ω	47 kΩ pull-up

Debug Probe Driver/Receiver (HS Whisker and AUTO26)

This chapter describes the actual driver/receiver circuit for debug signals inside the MIPI20T-HS Whisker and AUTO26 Debug Cable V2 and V3. For additional information, refer to the 74LVC1T45, NC7WB3125, MAX4616 and PCA6416A, data sheets. For the AUTO26 Debug Cable, all even-numbered pins are considered debug signals. For the HS whisker, even pins 2 to 10 are considered debug signals.



Input/Output Circuitry

Each signal uses a separate bidirectional level shifter. For the AUTO26 Debug Cable V2, two such level shifters are wired in parallel to the TCK signal, with one of them being only used as an input to provide a cable-internal return clock signal.

Dedicated Output Circuitry (only HS Whisker)

The MIPI20T-HS Whisker has bus switches wired in parallel to the input/output circuitry described above. At nominal debug VREF voltages up to 3.3 V, these are used for driving signals to the target instead of the level shifters.

Switchable Pull Resistors (only AUTO26 V2C)

Some pins have switchable pull resistors, implemented using a MAX4616 bus switch. The following table shows which pins have resistors and whether they are configured as pull-ups or pull-downs. The “always enabled” resistors are connected directly without a bus switch.

Pin	Signal	R	Direction
1	VREF-DEBUG	10 kΩ	down, always enabled
2	TMS	10 kΩ	down
4	TCK	10 kΩ	down
6	TDO	10 kΩ	down
8	TDI	10 kΩ	down
10	RESET-	10 kΩ	up
18	DBGRQ	10 kΩ	up
20	DBGACK	10 kΩ	up
24	BGRNT-	10 kΩ	up, always enabled

Switchable Pull Resistors (only AUTO26 V2E)

Some pins have switchable pull resistors, implemented using a MAX4616 bus switch. The following table shows which pins have resistors and whether they are configured as pull-ups or pull-downs. The “always enabled” resistors are connected directly without a bus switch.

Pin	Signal	R	Direction
1	VREF-DEBUG	10 kΩ	down, always enabled
2	TMS	10 kΩ	down
4	TCK	10 kΩ	down
6	TDO	10 kΩ	down
8	TDI	10 kΩ	down
10	RESET-	10 kΩ	up
12	RTCK	10 kΩ	up
18	DBGRQ	10 kΩ	up
20	DBGACK	10 kΩ	up
24	BGRNT-	10 kΩ	up, always enabled

Switchable Pull Resistors (only AUTO26 V3)

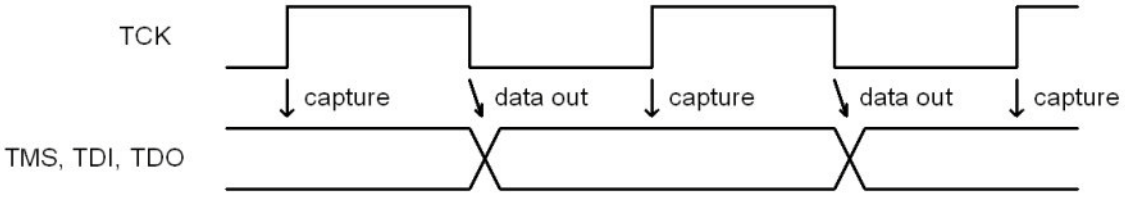
Some pins have switchable pull resistors, implemented using a common PCA6416A port expander. The port I/O supply of the expander is supplied by a buffered version of VREF. The following table shows which pins have resistors. The “always enabled” resistors are connected directly without using the port expander.

Pin	Signal	R	Direction
1	VREF	10 kΩ	down, always enabled
2	TMS	10 kΩ	up/down
4	TCK	10 kΩ	up/down
6	TDO	10 kΩ	up/down
8	TDI	10 kΩ	up/down
10	RESET-	10 kΩ	up/down
12	RTCK	10 kΩ	up/down

Pin	Signal	R	Direction
18	DBGRQ	10 kΩ	up/down
20	DBGACK	10 kΩ	up/down
24	BGRNT-	10 kΩ	up, always enabled

AC Electrical Characteristics

It is important for JTAG/cJTAG timing that the data on TDI and TMS is sampled on the rising edge of TCK (output on the falling edge) and that TDO changes on the falling edge of TCK. Other debug protocols have their own requirements.



All delays will affect the maximum possible JTAG frequency (TCK) which is selectable in the LAUTERBACH tool (default setting: 10 MHz). Problems with minimum setup and hold times can always be solved by simply decreasing the TCK frequency, since this increases the separation between the signal change and the sampling. Nevertheless you should keep the delays as low as possible to achieve good performance, e.g. when downloading the application program through the debugger.

The following table should give you an example for the JTAG timing considerations in case you want to work with a 20 MHz JTAG clock frequency, which results in a very good performance. Timing is measured at the connector of the probe operating in JTAG mode. Setup times and hold times are measured with respect to 50% signal level value, rise and fall times are measured at 20% and 80%. The measured values are for reference only and are not guaranteed by LAUTERBACH.

Symbol	Description	Min.	Max.	Unit
Ttck_high	TCK high time	22	28	ns
Ttck_low	TCK low time	22	28	ns
Tsetup	TDI, TMS setup time before rising TCK	21		ns
Thold	TDI, TMS hold time after rising TCK	21		ns
Ttdo_out	TDO output delay time from falling TCK	0	16	ns
Ttrst_low	TRST- low time	1		ms

Symbol	Description	Min.	Max.	Unit
Tsrst_low	RESET- low time	1		ms
Trf	output rise / fall time load = 10 pF load = 22 pF load = 33 pF		 6 7 8	ns

Values in table are for 20 MHz JTAG clock (TCK).

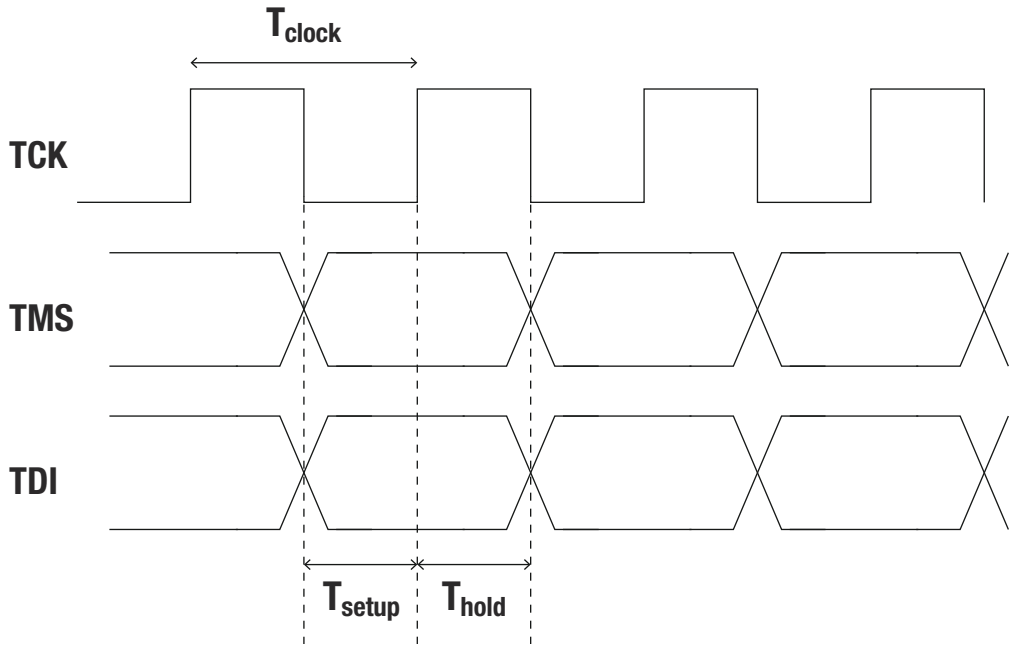
JTAG Timing

This document uses a simplified presentation of the timings (for example any kind of jitter and skew is ignored). This is reasonable because all timings depend on a configurable JTAG TCK clock frequency; to increase the margin to cover skew, jitter etc, simply use a lower JTAG TCK clock frequency.

For JTAG ports, the debugger sends three signals to the target chip for communication via JTAG:

- **TCK**: Clock signal, driven by the debugger.
- **TMS**: Signal driven by the debugger to control the JTAG TAP controller.
- **TDI**: Signal driven by the debugger to send data into the target chip.

The debugger changes the value of the **TMS** and **TDI** signals coincident to the falling edge of **TCK**. So the **TMS** and **TDI** signals have the following timing relative to **TCK**:

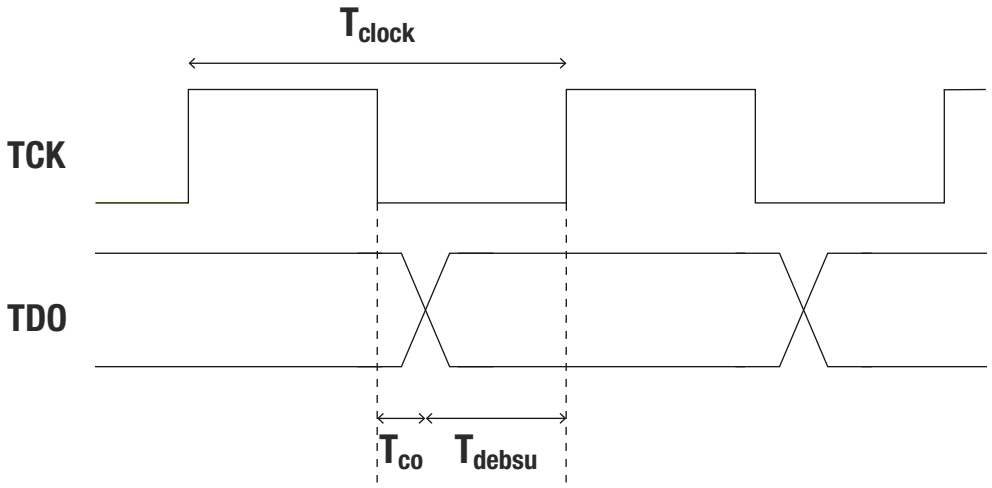


The target chip should sample the **TMS** and **TDI** signal on the rising edge of **TCK**.

For the target chip this means that the debugger will produce a setup (T_{setup}) and hold time (T_{hold}) of half the cycle time (T_{clock}) of **TCK**.

Example: At a **TCK** frequency of 1Mhz (T_{clock} = 1us), T_{setup} = 500ns and T_{hold} = 500ns.

The target chip drives the **TDO** signal. The value of the **TDO** signal should change after the falling edge of **TCK**. The target chip has an implementation dependent clock to output timing (T_{co}). The debugger per default samples the **TDO** signal on the rising edge of **TCK**:

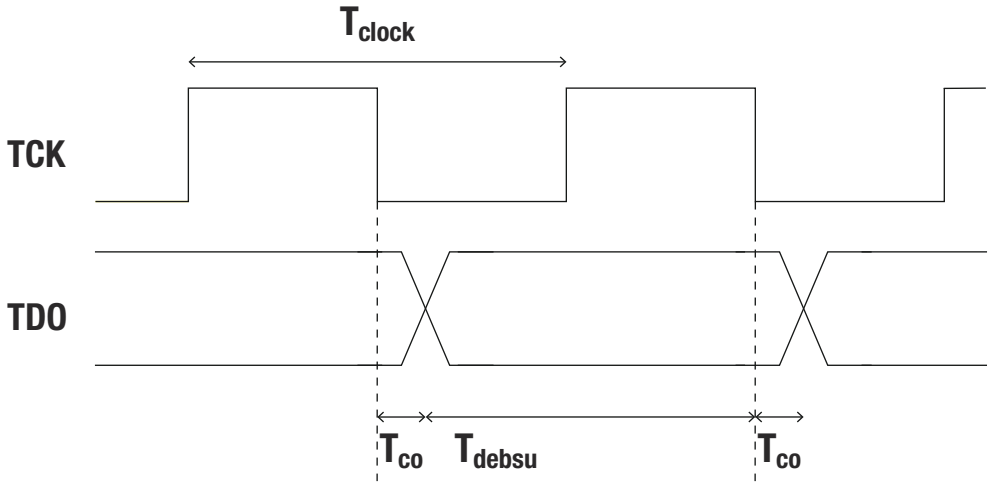


For the debugger this means the target chip will generate data on the **TDO** signal with a setup time of $T_{debsu} = T_{clock}/2 - T_{co}$. The hold time of the data will be $T_{co} + T_{clock}/2$.

Example: At a **TCK** frequency of 1MHZ (T_{clock} = 1us) and T_{co} = 10ns, T_{debsu} = 490ns.

The debugger has the requirement that $T_{co} + T_{clock}/2 > 0$ns (hold time requirement) and $T_{debsu} > 7.5$ns (setup time requirement).

To achieve higher **TCK** frequencies (which means lower T_{clock} values), the debugger offers the option to sample the **TDO** signal on the falling edge of **TCK**. In this case the following figure explains the timing:



So in this case the target generates a setup time for the debugger of $T_{debsu} = T_{clock} - T_{co}$. The debugger still has a 0 ns hold time requirement, so in this case it must hold that $T_{co} > 0$ns.

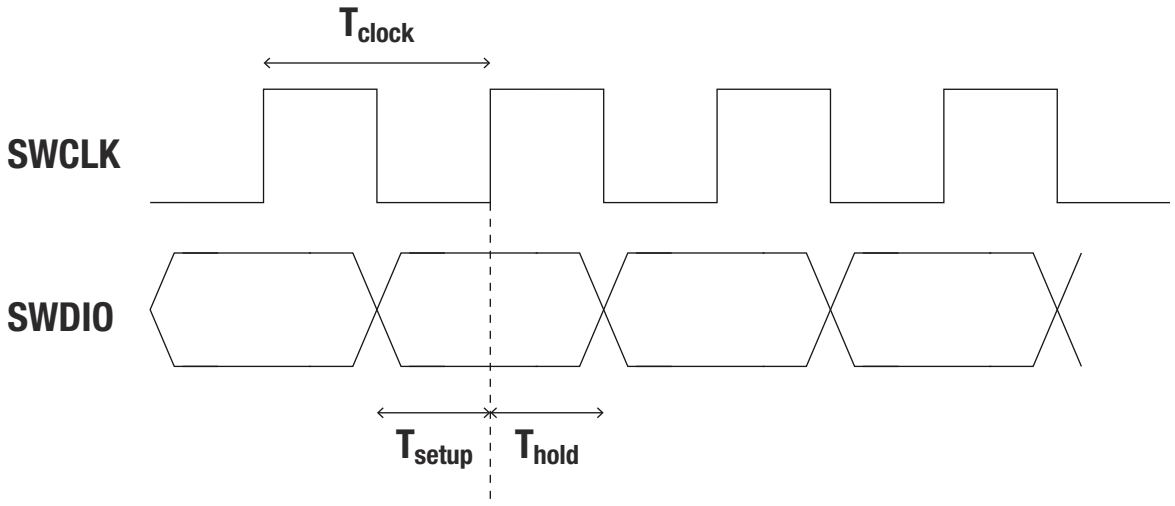
SWD Timing

This document uses a simplified presentation of the timings (for example any kind of jitter and skew is ignored). This is reasonable because all timings depend on a configurable debug clock frequency; to increase the margin to cover skew, jitter etc, simply use a lower debug clock frequency.

In Serial Wire Debug mode, only two signals are used to communicate with a target chip:

- **SWCLK**: Clock signal, driven by the debugger.
- **SWDIO**: Bidirectional data signal driven by both the debugger and the target chip.

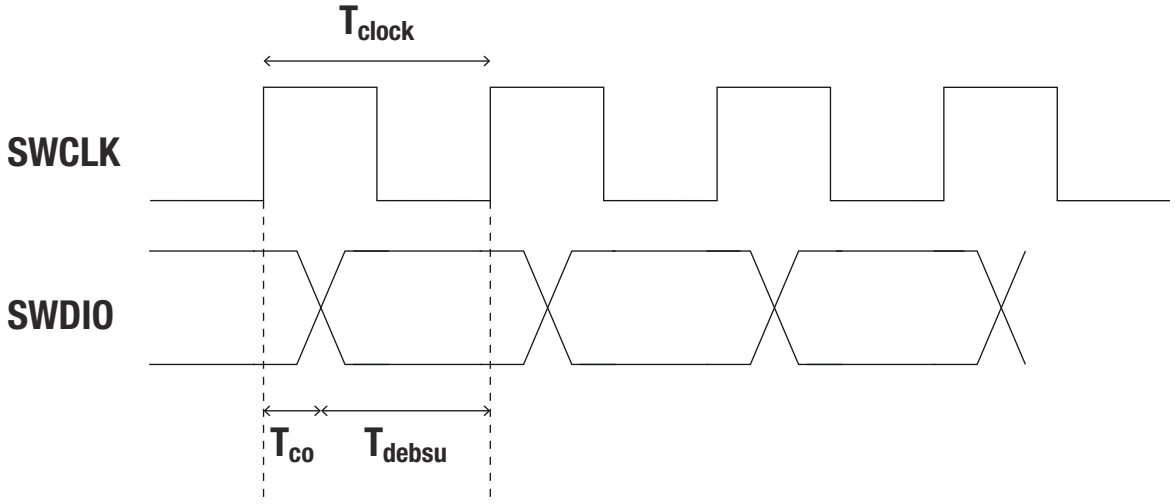
When the debugger drives the SWDIO line, the debugger changes the value of SWDIO incident to the falling edge of SWCLK.



For the chip this means that the debugger will produce a setup (T_{setup}) and hold time (T_{hold}) of half the cycle time (T_{clock}) of **SWCLK**.

Example: At a frequency for **SWCLK** of 1Mhz (T_{clock} = 1us), T_{setup} = 500ns and T_{hold} = 500ns.

If the target chip drives the **SWDIO** line, the value of the SWDIO line should change after the rising edge of **SWCLK**. The target chip has an implementation dependent clock to output timing (T_{co}):

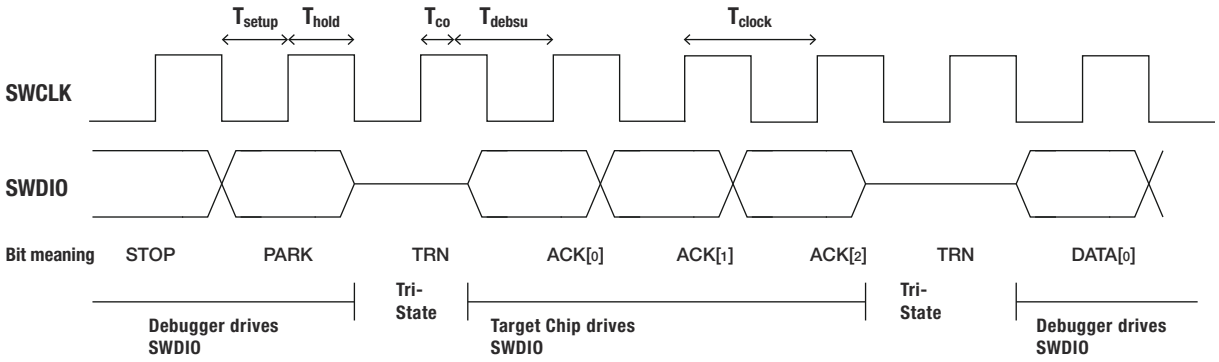


For the debugger this means that the target chip will generate data on the **SWDIO** signal with a setup time of $T_{debsu} = T_{clock} - T_{co}$. The hold time of the data will be at least T_{co}.

Example: At a frequency for **SWCLK** of 1MHZ (T_{clock} = 1us) and T_{co} = 2ns, T_{debsu} = 998ns.

The debugger has the requirement that T_{co} > 0ns (hold time requirement) and T_{debsu} > 7.5ns (setup time requirement).

Here is an extract out of a Serial Wire Debug write transaction that shows the timing for the turn around periods, in which the **SWDIO** line is tri-stated (when the drive of SWDIO is turned around).



Target Design Considerations

Electrical

The debug interfaces are not fault tolerant. A spike on the TCK/TMSC/SWCLK clock will most likely cause communication to fail, requiring a re-initialization of the debug interface and a restart of the debug session. Therefore, careful interface design is required to ensure that the debugger works stably.

A direct and short connection (no buffer or level shifter) between the probe connector and the processor is recommended.

The debugger output signals are serially terminated to reduce signal reflections. Accordingly, you can provide a 47 Ω series resistor near the processor for the serial termination on the TDO line (JTAG) or SWDIO and SWO line (SWD) or TMSC line (cJTAG), if the chip's output driver are not impedance matched.

RTCK is not required and should not be used/connected. A direct connection to TCK (JTAG) leads to a stub on the TCK line and causes a signal problem that we often see on customer boards.

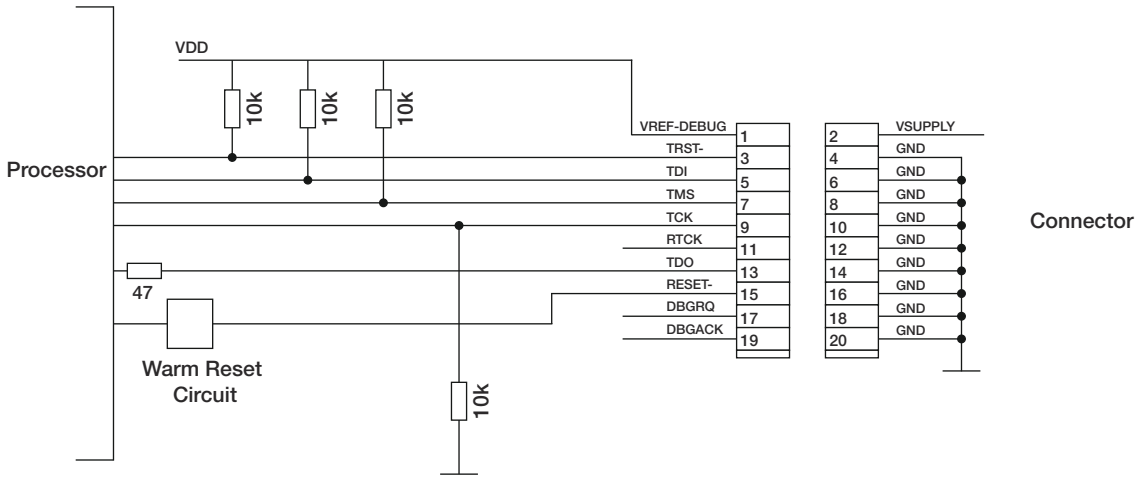
Note that TMS (JTAG) becomes bidirectional when used for TMSC (cJTAG) or SWDIO (SWD). Do not use a unidirectional driver in this case.

Optional, unused signals can be left open (recommended). If you apply a fixed level to an optional unused terminal you must use the inactive state: RTCK = low, DBGRQ = low, DBGACK = low, TRST- = high, RESET- = high.

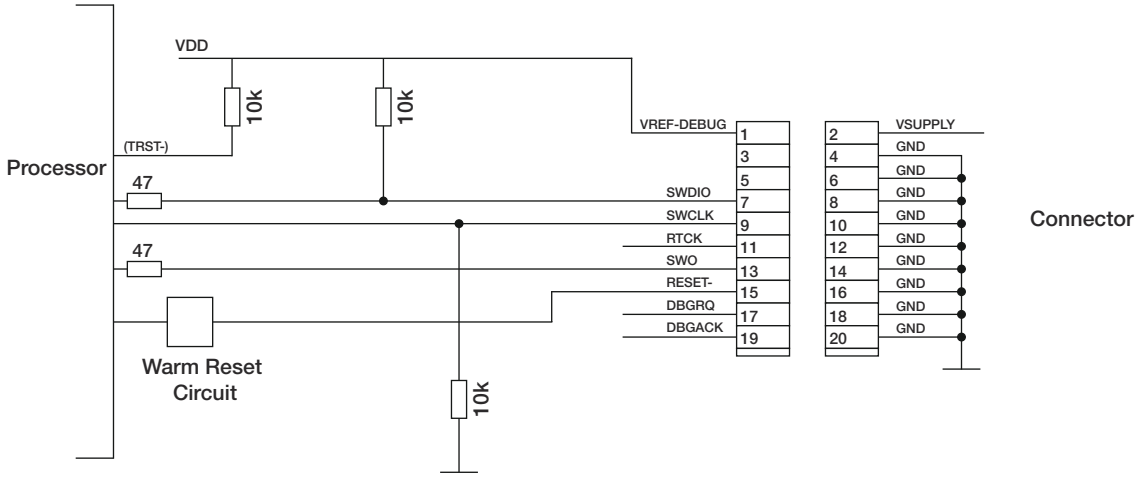
The recommended pull-up/pull-down value is 10 kΩ (1 kΩ - 47 kΩ). Pull-up or pull-down resistors can be used to give signals a defined level when the debugger is disconnected or tristated. This also reduces crosstalk on the cable between the debugger and the connector.

There are more design notes for each signal in the **Debug Signals** chapter.

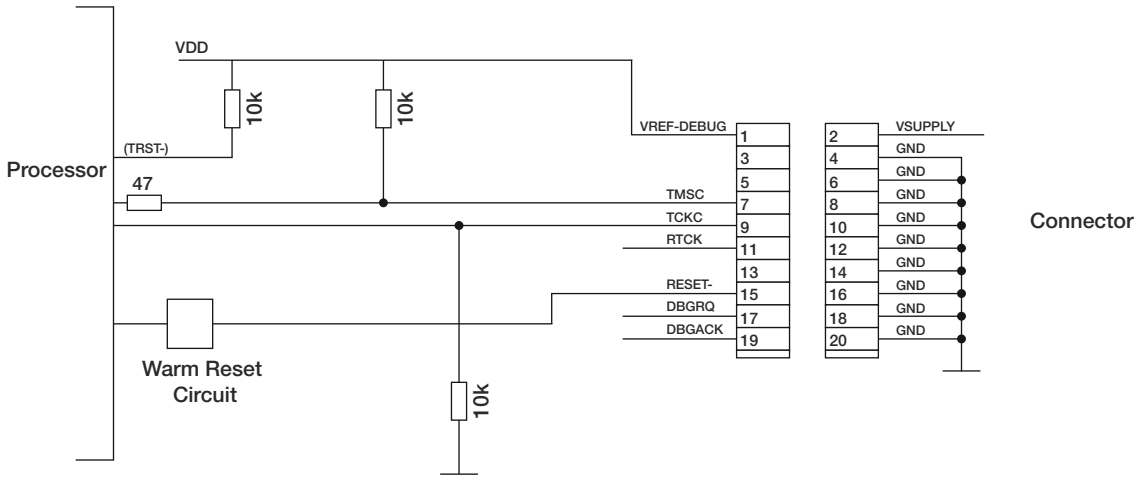
Example for a JTAG Interface on the Target Board



Example for a SWD Interface on the Target Board



Example for a cJTAG Interface on the Target Board



- **Ensure adequate space around the connector to accommodate the insertion of the debug probe.**

  We recommend using connectors with housing to minimize the risk of incorrect connections. Additionally, it's advisable to avoid placing tall components near the connector.

- **Position the trace connector close to the chip for optimal performance.**

  For the trace interface connector, maintain an even shorter distance, preferably less than 2 inches.

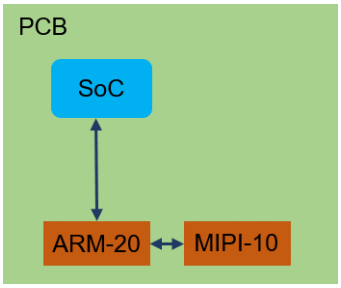
- **Position the connector at the edge of the PCB to facilitate probe insertion.**

  However, for a trace connector, proximity to the chip is more important.

- **Do not connect the debug signal to the trace connector when using a separate debug connector.**

  This avoids stubs at the debug signals.

- **If supplying multiple connectors with debug signals on the target, adhere to the following guidelines.**



  - The connectors should be placed as close together as possible (as shown in the above drawing).

  - Avoid long stub lines at junctions.

  - If you have more than one SoCs on your board and are daisy-chaining them via JTAG, we recommend using the Lauterbach daisy-chainer. You can find more information at **www.lauterbach.com/jtag_switcher.html**.

In addition to the general recommendations, there are also recommendations for the individual connectors.

- For ARM-20 refer to **“ARM-20”**, page 17.
- For MIPI-20T refer to **“MIPI-20T”**, page 18.
- For MIPI-10 refer to **“MIPI-10”**, page 19.
- For AUTO-26 refer to **“AUTO-26”**, page 20.
- For Mictor-38 refer to **“Mictor-38”**, page 47.
- For MIPI-60 refer to **“MIPI-60”**, page 49.
- For Samtec-40 refer to **“Samtec-40”**, page 52.

Reset Considerations

RESET- versus TRST-

For debugging purposes, the two reset lines must be treated independently:

TRST-: Resets the JTAG or SWD TAP controller and possibly the CPU internal debug logic.

RESET-: Resets the CPU core and peripheral modules. This reset should only be a warm reset. A true power-on reset puts everything on the chip in a defined reset state, including the debug interface. However, you want the debug interface to remain operational.

If this is not the case, you will encounter problems in the following two scenarios:

Debugging from the Very Beginning

The standard sequence to start a debug session is:

- assert TRST- and RESET-
- de-assert TRST- (debug communication can begin)
- initialize the debug logic via JTAG/SWD and send a break request
- de-assert RESET- (processor becomes active and starts executing the program)
- break request takes immediate effect, breaks before the first instruction is executed

This scenario provides debug control from the very first instruction of the application code.

Problems occur when TRST- is connected directly to RESET-. The debugger cannot send the break request before RESET- is released. As a result, the processor starts executing the program and some of the boot code is executed before a break request can take effect. Even if you set the program counter to the reset value, the debug session no longer reflects the actual behavior of the program because peripherals and interrupts may already be initialized.

If this situation cannot be avoided due to an existing design, the following work arounds may help:

- Set an endless loop to the reset vector and disable the watchdog there if necessary. After startup, load your program and set the program counter from the endless loop to the beginning of your program.
- There may be a way to soft reset the processor. This could be done after the startup procedure to put the processor in reset state. This assumes that the softreset does not trigger a TRST- like reset.

Debugging a Reset Event

Debugging a reset event is generally supported. Problems occur when this reset event

- forces a reset of the JTAG/SWD-TAP controller, because this terminates the communication between the debugger and the processor
- forces a reset of the debug registers, e.g. on-chip breakpoints, as these then become inactive

In either case, the debugging session must be restarted.

Hot Plugging

The JTAG connector of the debug cable is not suitable for hot plugging. It is uncertain which signals will make contact first. Connecting all the uncharged signals may cause glitches. In particular, there is a risk of triggering a reset at RESET-. You may be lucky if RESET- is not connected.

To solve this problem, a special adapter may be required that first connects the ground of the debugger and the target. Then, a voltage is applied to the reference voltage pin (VREF-DEBUG) to pre-charge the signals. In particular, the reset signal (RESET-) will be high at the moment of connection.

Trace Interface

This refers to all trace interfaces that require additional off-chip signals. A distinction is made between Parallel Trace (TPIU), Serial Trace (Aurora, HSSTP) and PCIe Trace.

Parallel Trace Interface

The parallel trace interface, which is fed by Arm's Trace Port Interface Unit (TPIU), consists mainly of a trace clock (TRACECLK) and up to 32 trace data signals (TRACEDATA[0..31]) as well as an optional trace control signal (TRACECTL).

Parallel Trace Connector

Mictor-38

This connector is the default connector of our **AutoFocus II Preprocessor**. You only need the second connector if your trace port width is > 16 bits.

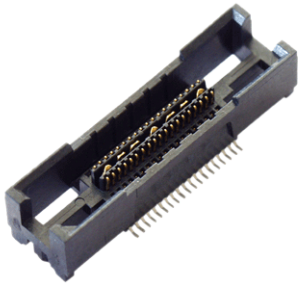
Pinout Connector 1:

Signal	Pin	Pin	Signal
N/C	1	2	N/C
N/C	3	4	N/C
GND	5	6	TRACECLK
DBGRQ	7	8	DBGACK
RESET-	9	10	EXTRIG
TDOI-ISWO	11	12	VREF-TRACE
RTCK	13	14	VREF-DEBUG
TCKITCKCISWCLK	15	16	TRACEDATA[7]
TMSITMSCISWDIO	17	18	TRACEDATA[6]
TDI	19	20	TRACEDATA[5]
TRST-	21	22	TRACEDATA[4]
TRACEDATA[15]	23	24	TRACEDATA[3]
TRACEDATA[14]	25	26	TRACEDATA[2]
TRACEDATA[13]	27	28	TRACEDATA[1]
TRACEDATA[12]	29	30	GND
TRACEDATA[11]	31	32	GND
TRACEDATA[10]	33	34	VCC
TRACEDATA[9]	35	36	TRACECTL
TRACEDATA[8]	37	38	TRACEDATA[0]

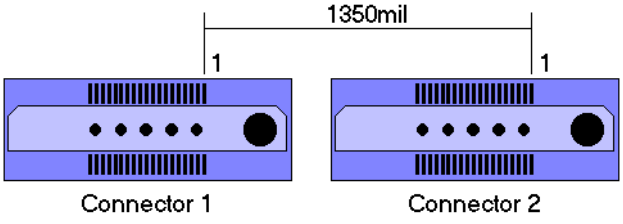
Pinout Connector 2:

Signal	Pin	Pin	Signal
N/C	1	2	N/C
N/C	3	4	N/C
GND	5	6	N/C
N/C	7	8	N/C
N/C	9	10	N/C
N/C	11	12	N/C
N/C	13	14	N/C
N/C	15	16	TRACEDATA[23]
N/C	17	18	TRACEDATA[22]
N/C	19	20	TRACEDATA[21]
N/C	21	22	TRACEDATA[20]
TRACEDATA[31]	23	24	TRACEDATA[19]
TRACEDATA[30]	25	26	TRACEDATA[18]
TRACEDATA[29]	27	28	TRACEDATA[17]
TRACEDATA[28]	29	30	GND
TRACEDATA[27]	31	32	GND
TRACEDATA[26]	33	34	VCC
TRACEDATA[25]	35	36	GND
TRACEDATA[24]	37	38	TRACEDATA[16]

Target Connector:



Placement:



A separation distance of 1350 mils is required for adaptation without flex cable or for optimum routing of the flex cables. We recommend placing the even numbered pins on the edge of the board (probe flex cable won't get twisted). More important for signal quality, however, is placing the trace connector close to the processor.

Example: Tyco 2-5767004-2 or 767054-1 or 767061-1 (vertical, surface mount), Tyco 5767044-1 (right angle, straddle mount)

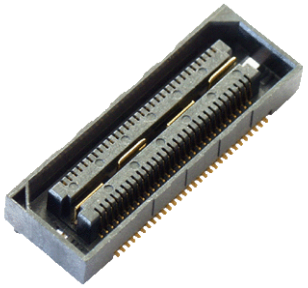
MIPI-60

This connector is the default connector of our **AutoFocus II MIPI Preprocessor**. The connector can be found on evaluation boards from Texas Instruments. The advantage is you have just one connector even if the trace port is > 16-bit wide. The disadvantage is that the connection is less robust. Therefore we do not recommend to use this connector for new board designs. Use **Mictor-38** instead.

Pinout:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
TCK|TCKC|SWCLK	3	4	TDO|-|SWO
TDI	5	6	RESET-
RTCK	7	8	TRST- PULLDOWN
TRST-	9	10	DBGRQ TRIGIN
DBGACK TRIGOUT	11	12	VREF-TRACE
TRACECLK	13	14	GND
GND	15	16	GND
TRACECTL	17	18	TRACEDATA[19]
TRACEDATA[0]	19	20	TRACEDATA[20]
TRACEDATA[1]	21	22	TRACEDATA[21]
TRACEDATA[2]	23	24	TRACEDATA[22]
TRACEDATA[3]	25	26	TRACEDATA[23]
TRACEDATA[4]	27	28	TRACEDATA[24]
TRACEDATA[5]	29	30	TRACEDATA[25]
TRACEDATA[6]	31	32	TRACEDATA[26]
TRACEDATA[7]	33	34	TRACEDATA[27]
TRACEDATA[8]	35	36	TRACEDATA[28]
TRACEDATA[9]	37	38	TRACEDATA[29]
TRACEDATA[10]	39	40	TRACEDATA[30]
TRACEDATA[11]	41	42	TRACEDATA[31]
TRACEDATA[12]	43	44	GND
TRACEDATA[13]	45	46	GND
TRACEDATA[14]	47	48	GND
TRACEDATA[15]	49	50	GND
TRACEDATA[16]	51	52	GND
TRACEDATA[17]	53	54	GND
TRACEDATA[18]	55	56	GND
GND	57	58	GND
GND	59	60	GND

Target Connector:



Placement:

We recommend placing the odd numbered pins on the edge of the board (probe flex cable won't get twisted). More important for signal quality, however, is placing the trace connector close to the processor.

Example: Samtec QSH-030-01-L-D-A

Signal / Direction	Description	Compliance	Recommen-dation
EXTRIG from/to debugger	“External Trigger” this signal is not (yet) used by the debugger. It can be an input or output.	Not used.	Do not connect.
GND	“Ground”. Do not forget to connect the ground plane in the middle of the Mictor connector.	Required.	
TRACE CLK to debugger	“Trace Clock” to capture a data value at the trace data port.	Required.	
TRACE CTL to debugger	“Trace Control”. It indicates that the trace port is idle. If this signal is not used (continuous mode), then the information is wrapped in the trace data protocol.	Optional.	Connect directly to GND if not used.
TRACE DATA [0..31] to debugger	“Trace Data”. Up to 32 parallel data bits are possible. If you use more than 16, you need a second Mictor connector, which is otherwise not required.	Required.	Connect unused data pins directly to GND.
VCC	This terminates trace port analyzer input pins which are not used here. The level shall be as VREF-TRACE. It may not be connected to a weak VREF-TRACE (if provided via serial resistor), because this pin draws some milli-amps and would drop the voltage level if the probe termination is used.	Not used.	Should be connected.
VREF-TRACE to debugger	“Voltage Reference Trace” is the target reference voltage for the trace signals.	Required.	

N/C', 'Not Connected' rather means that this pin should not be connected on the target board.

For other signals in the pin assignment, see the description of the **Debug Signals**. They are only required if you also want to use the trace connector for debugging. If you have a separate debug connector on the target board, it is recommended that you do not connect these signals to the trace port (leave them unconnected) to avoid stubs on the debug signals.

For more information, such as electrical characteristics and target board design recommendations, refer to the **"Arm ETM Trace"** (trace_arm_etm.pdf) and the **"AutoFocus User's Guide"** (autofocus_user.pdf).

Serial Trace Interface

The serial trace interface consists of 1 to 6 serial lanes TXP/TXN[0..6] (differential line pairs) using the Aurora/HSSTP protocol.

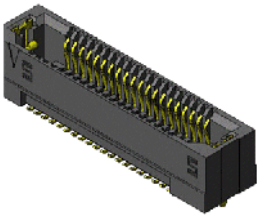
Serial Trace Connector

Samtec-40

Pinout:

Signal	Pin	Pin	Signal
TXP[4]	1	2	VREF-DEBUG
TXN[4]	3	4	TCK|TCKC|SWCLK
GND	5	6	GND
TXP[2]	7	8	TMS|TMSC|SWDIO
TXN[2]	9	10	TRST-
GND	11	12	GND
TXP[0]	13	14	TDI
TXN[0]	15	16	TDO|-|SWO
GND	17	18	GND
CLKP	19	20	RESET-
CLKN	21	22	DBGRQ
GND	23	24	GND
TXP[1]	25	26	DBGACK
TXN[1]	27	28	RTCK
GND	29	30	GND
TXP[3]	31	32	TRIGIN
TXN[3]	33	34	TRIGOUT
GND	35	36	RESERVED
TXP[5]	37	38	RESERVED
TXN[5]	39	40	RESERVED

Target Connector:



Placement:

We recommend placing the even numbered pins on the edge of the board (probe flex cable won't get twisted). More important for signal quality, however, is placing the trace connector close to the processor.

Example: Samtec ASP-130367-01

Signal / Direction	Description	Compliance	Recommen-dation
CLKP/ CLKN from debugger	“Clock.”. A differential line pair from the debugger to the target that provides a reference clock for the trace data transmitter.	Optional.	Use when there is no other suitable clock source on the target.
GND	“Ground”.	Required.	
RE SERVED		Not used.	Do not connect.
TRIGIN to debugger	“Trigger Input”. This is an input line that can currently stop the trace recording on a rising edge. Perhaps there will be more functions behind it in the future.	Optional.	Do not connect if you do not have a need for it.
TRIGOUT from debugger	“Trigger Output”. This is a signal on which the debugger can output a trigger signal. This is reserved for future use rather than having a specific function behind it.	Optional, no concrete purpose assigned yet.	Do not connect.
TXP/ TXN[0..6] to debugger	“Transmit Positive / Transmit Negative”. Differential line pairs that transfer the trace data.	Required, at least one pair.	Connect the lanes starting with the number 0, then in ascending order. Leave unused lanes unconnected.

For other signals in the pin assignment, see the description of the **Debug Signals**. They are only required if you also want to use the trace connector for debugging. If you have a separate debug connector on the target board, it is recommended that you do not connect these signals to the trace port (leave them unconnected) to avoid stubs on the debug signals.

For more information, including electrical characteristics and target board design recommendations, refer to the **“PowerTrace Serial User’s Guide”** (serialtrace_user.pdf).

PCIe Trace Interface

The PCIe trace interface uses a standard PCIe memory interface. As a prerequisite a PCIe root complex is running on the chip. The debugger is connected to it and emulates a memory. The trace data is saved in this memory location. This is usually done by the Embedded Trace Router (ETR) or the Embedded Trace Streamer (ETS) module from Arm on the chip.

PCIe Trace Connector

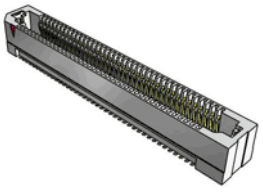
Samtec-80

This connector can be used directly on the target board. However, it is more typical to have a standard PCIe connector on the target and to use a suitable slot card converter (see **"LAUTERBACH Probe Description"**, page 11). See the industry standard for these connectors, pinout and signal description.

Pinout:

Signal	Pin	Pin	Signal
GND	1	2	GND
PETP[0]	3	4	PERP[0]
PETN[0]	5	6	PERN[0]
GND	7	8	GND
PETP[1]	9	10	PERP[1]
PETN[1]	11	12	PERN[1]
GND	13	14	GND
PETP[2]	15	16	PERP[2]
PETN[2]	17	18	PERN[2]
GND	19	20	GND
PETP[3]	21	22	PERP[3]
PETN[3]	23	24	PERN[3]
GND	25	26	GND
PETP[4]	27	28	PERP[4]
PETN[4]	29	30	PERN[4]
GND	31	32	GND
PETP[5]	33	34	PERP[5]
PETN[5]	35	36	PERN[5]
GND	37	38	GND
PETP[6]	39	40	PERP[6]
PETN[6]	41	42	PERN[6]
GND	43	44	GND
PETP[7]	45	46	PERP[7]
PETN[7]	47	48	PERN[7]
GND	49	50	GND
WAKE#	51	52	REFCLK+
PWRGOOD	53	54	REFCLK-
GND	55	56	GND
RESERVED	57	58	RESERVED
RESERVED	59	60	RESERVED
VCC3V3	61	62	VCC3V3
RESERVED	63	64	RESERVED
RESERVED	65	66	RESERVED
VCC3V3	67	68	VCC3V3
RESERVED	69	70	GND
RESERVED	71	72	RESERVED
VCC3V3	73	74	VCC3V3
RESERVED	75	76	RESERVED
RESERVED	77	78	VCCSENSE
VCC3V3	79	80	VCC3V3

Target Connector:



Placement:

We recommend placing the even numbered pins on the edge of the board (probe flex cable won't get twisted). More important for signal quality, however, is placing the trace connector close to the processor.

Example: Samtec ERF8-040-05.0-S-DV-L-TR

PCIe Trace Signals

Signal / Direction	Description	Compliance	Recommen-dation
GND	“Ground”. Pin 70, is not GND on the debugger side. Instead, it is used to detect if a target is connected. If it is, the debugger will apply voltage to the VCC3V3 pins.	Required.	Connect them all to GND, including pin 70. Also connect the latch pins (mechanical locking) of the connector to GND.
PERP/ PERN [0..7], PETP/ PETN [0..7] from/to debugger	“PCI Express Receiver Positive/Negative”, “PCI Express Transmitter Positive/Negative”: The PETP and PETN pins must be connected to the PCIe Express Transmitter differential pair on the target system board. They are connected to the differential pair of the PCI Express Receiver on the trace tool. The PERP and PERN pins must be connected to the PCIe Express Receiver differential pair on the target system board. They are connected to the PCI Express Transmitter differential pair on the trace tool. The AC coupling (220nF) is already done on the tool side, so no caps are needed on the target side.	Required.	
PWR GOOD from/to debugger	“Trigger Input”. This is an input line that can currently stop trace recording on a rising edge. Perhaps there will be more functions behind it in the future.	Required, needs to have 3.3V level.	
REFCLK +/REFCL K- to debugger	“Trigger Output”. This is a signal for which the debugger can output a trigger signal. This is reserved for future use rather than having a specific function behind it.	Required.	
RE SERVED	Connected on the tool side for a purpose not needed here.	Not needed.	Do not connect.

Signal / Direction	Description	Compliance	Recommen-dation
VCC3V3 from debugger	3.3V Supply Voltage: Power supplied by the tool. It can be used to power pull-up resistors if there is no 3.3V supply on the target to bring the level of the WAKE, POWERGOOD, VCCSENSE signal to the correct (3.3V) level.	Optional.	Do not connect if you do not need it.
VCC SENSE to debugger	Target Voltage Sense. It represents the voltage level of the WAKE and POWERGOOD signals, which must be 3.3 V.	Optional.	Connect it.
WAKE# from debugger	Wake-up Request Signal. Requires a 3.3 V level.	Optional, currently not used by the debugger.	Connect it for future use if available, otherwise do not connect it.

For more information, such as electrical characteristics and target board design recommendations, refer to the **"PowerTrace Serial User's Guide"** (serialtrace_user.pdf).

Converter

Sometimes the connector on the target does not match the standard connector on the probe. For common use cases we offer cross converters.

MIPI-34, supported by the former CombiProbe probe, and MIPI-20D, supported by the former CombiProbe and AUTO-26 probes, are not relevant as a target interface and are therefore not described here.

However, MIPI-34 is still used in some of our tools (PowerTrace Serial 2, AutoFocus II MIPI Preprocessor) to connect a debug probe to the trace module when a common debug and trace connector is to be used on the target. MIPI-34 and suitable converters are also shown in the table below.

Cross Converting Table

From To	ARM-20	MIPI-20T MIPI-10	AUTO-26 MIPI-20T MIPI-10	Mictor-38	MIPI-60
ARM-20 HSSTP Pre. AF II Pre.	native	**LA-2730**	**LA-2730**	useless	useless
MIPI-10	**LA-3809 LA-3770**	native	native	useless	useless
MIPI-20T	**LA-3809** (**LA-3770** 1))	native	native 2)	**LA-3809**	not available (**LA-3817**+ **LA-3809**)
Mictor-38	**LA-3722** (**LA-3862**)	**LA-2776**	**LA-2776**	native	**LA-3817 LA-3880** (>16-bit)
MIPI-60	**LA-3818**	**LA-2775**	**LA-2775**	**LA-3818**	native
MIPI-34 on AF II MIPI Pre.	**LA-3770** (**LA-2770**)	**LA-2774**	**LA-2774**	useless	useless
MIPI-34 on PTSerial 2, Aurora 2 Pre.	**LA-2770** (**LA-3770**)	**LA-2774**	**LA-2774**	useless	useless

LA-???? is the LAUTERBACH order number for this converter.
1) Open the solder bridges J101, J102 on the converter.
2) Use the “SYStem.CONFIG.CONNECTOR Auto10-ARM” debugger setting.

Cross Converting Table for Manufacturer Specific Connectors

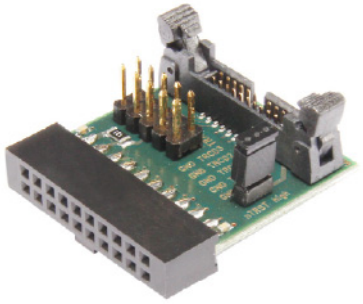
Some chip manufacturers have their own proprietary debug connectors on their target boards. Converters are available for some of these connectors, making it easy to use their evaluation boards. The table below lists the most important ones. For custom target board designs, it is recommended to use the standard connectors described in the previous chapters.

From To	ARM-20	MIPI-20T MIPI-10	AUTO-26 MIPI-20T MIPI-10
TI-14	**LA-7748**	**LA-2777**	**LA-2777**
TI-20-Compact	**LA-3780**	not available	not available
Altera-10	**LA-3863**	not available	not available
Xilinx-14	**LA-3881**	not available	not available

Converter Description

LA-2730 Converter MIPI-20T to IDC20A

The purpose of this converter is to connect the debug signals of a MIPI20T-HS Whisker (on a CombiProbe 2 or µTrace) to a target with an ARM-20 connector. It also includes a pin header to connect the signals of a 4-bit wide parallel trace interface to the target, if present.

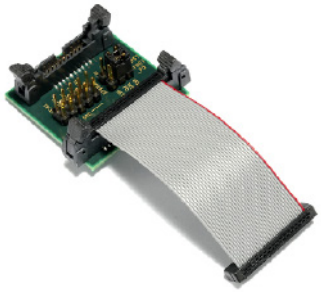


MIPI-20T Connector
ARM-20 Connector
Debug Signal Description

LA-2770 Converter IDC20A to MIPI-34 PowerTrace Serial

See **LA-3770**.

It can be used to connect only the debug signals of a MIPI-20T probe (of a CombiProbe 2 or µTrace or AUTO-26 probe) to an AutoFocus II MIPI Preprocessor or a PowerTrace Serial 2 or Aurora 2 Preprocessor.

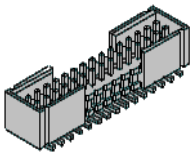


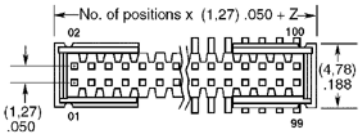
MIPI-20T Connector
Debug Signal Description

Pinout MIPI-34:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
GND	3	4	TCK|TCKC|SWCLK
GND	5	6	TDO|-|SWO
GND (KEY)	-	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	TRST- PULLDOWN
GND	15	16	TRST-
GND	17	18	DBGRQ (EMU0)
GND	19	20	DBGACK (EMU1)
GND	21	22	TRACECLK
GND	23	24	TRACEDATA[0]
GND	25	26	TRACEDATA[1]
GND	27	28	TRACEDATA[2]
GND	29	30	TRACEDATA[3]
GND	31	32	TRACEEXT
GND	33	34	VREF-TRACE

Target Connector:





The target board requires a 34 pin double row male connector with 1.27mm/0.050" x 1.27mm/0.050" pin to pin spacing and 0.016" square post width. A shrouded connector with center polarization is recommended. Pin 7 is a key pin that prevents mating in the wrong orientation. Therefore, pin 7 must be removed on the target side.

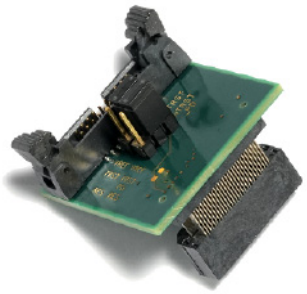
Placement:

We recommend placing the odd numbered pins on the edge of the board (probe flex cable won't get twisted).

Example with housing: Samtec FTSH-117-01-L-DV-K (surface mount)

LA-2775 Converter MIPI-20T to MIPI-60

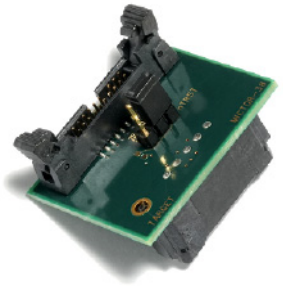
Converter for connecting a MIPI-20T probe (from a CombiProbe 2 or µTrace or AUTO-26 probe) to a target with a MIPI-60 connector. It can be used for debugging and optionally for 4-bit parallel tracing if the bandwidth is sufficient (only with CombiProbe 2 or µTrace).



MIPI-20T Connector
MIPI-60 Connector
Debug Signal Description
Parallel Trace Signal Description

LA-2776 Converter MIPI-20T to MICTOR-38

Converter for connecting a MIPI-20T probe (from a CombiProbe 2 or µTrace or AUTO-26 probe) to a target with a Mictor-38 connector. It can be used for debugging and optionally for 4-bit parallel tracing if the bandwidth is sufficient (only with CombiProbe 2 or µTrace).



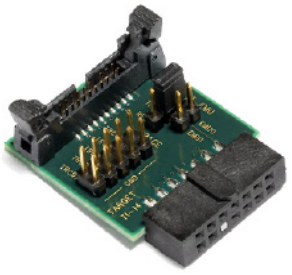
MIPI-20T Connector
Mictor-38 Connector
Debug Signal Description
Parallel Trace Signal Description

LA-2777 Converter MIPI-20T to TI-14

This connector is defined by Texas Instruments and is used on many of their target boards.

The converter can be used to connect only the debug signals of a MIPI-20T probe (from a CombiProbe 2 or µTrace or AUTO-26 probe) to a TI-14 connector on the target. A pin header allows the 4-bit trace port to be connected to the target, if present on the target (only with CombiProbe 2 or µTrace).

The TI-14 connector does not provide the RESET- signal. TRST- is connected to VREF-DEBUG by a jumper. EMU0 and EMU1 are not used but can be connected via a pin header. EMUx are signals from Texas Instruments processors for additional programmable debug features.

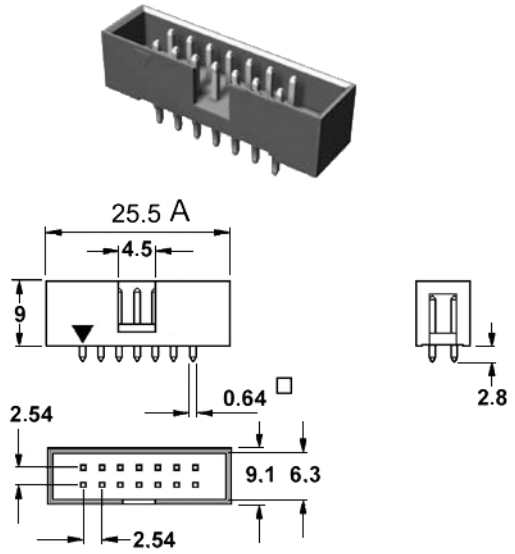


MIPI-20T Connector
Debug Signal Description

Pinout TI-14:

Signal	Pin	Pin	Signal
TMS|TMSC|SWDIO	1	2	TRST-
TDI	3	4	GND
VREF-DEBUG	5	-	GND (KEY)
TDO|-|SWO	7	8	GND
RTCK	9	10	GND
TCK|TCKC|SWCLK	11	12	GND
EMU0	13	14	EMU1

Target Connector:



The target board requires a standard 14 pin double row male connector, pin to pin spacing 2.54mm/0.100" x 2.54mm/0.100" and 0.025" square post width. A shrouded connector with center polarization is recommended. Pin 6 of the converter's female connector is plugged to prevent incorrect connection. Therefore, remove the terminal from pin 6 of the target connector. If a terminal block without a cover is used, the space marked “A” must be a minimum of 23mm/0.9”.

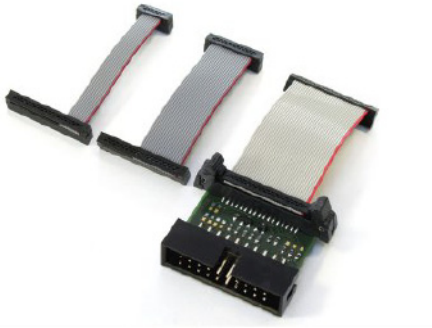
Examples with housing: Samtec HTST-107-01-L-D (through-hole), Samtec HTST-107-01-L-DV (surface mount)

Examples without housing: Samtec TSW-107-23-L-D, Berg: 67996-114H

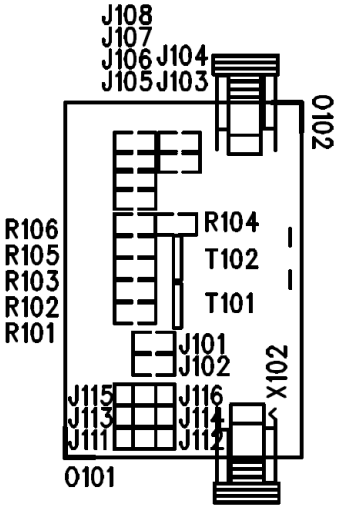
LA-3722 Converter IDC20A to Mictor-38

See **LA-3862**.

LA-2770 is identical to LA-3770, but comes with a MIPI-34 ribbon cable only, and has the connector positioning reversed to provide a smoother connection for PowerTrace Serial 2 or Aurora 2 Preprocessor. The LA-3770 is the preferred option for all other cases and is described below.



If you are using the converter with MIPI-20T, you must open J101 and J102 (and J103, which is open by default) on the converter. This is especially important if something is connected to pin 14 or pin 16 (or pin 18 on the target board). While it may still work without opening these jumpers, there may be output driver conflicts that should be avoided even though the current is limited by a serial resistor.

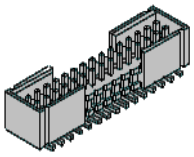


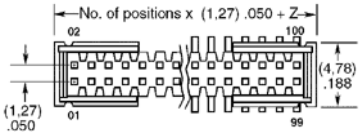
ARM-20 Connector
MIPI-10 Connector
MIPI-20T Connector
Debug Signal Description

Pinout MIPI-34:

Signal	Pin	Pin	Signal
VREF-DEBUG	1	2	TMS|TMSC|SWDIO
GND	3	4	TCK|TCKC|SWCLK
GND	5	6	TDO|-|SWO
GND (KEY)	-	8	TDI
GND	9	10	RESET-
GND	11	12	RTCK
GND	13	14	TRST- PULLDOWN
GND	15	16	TRST-
GND	17	18	DBGRQ (EMU0)
GND	19	20	DBGACK (EMU1)
GND	21	22	TRACECLK
GND	23	24	TRACEDATA[0]
GND	25	26	TRACEDATA[1]
GND	27	28	TRACEDATA[2]
GND	29	30	TRACEDATA[3]
GND	31	32	TRACEEXT
GND	33	34	VREF-TRACE

Target Connector:





The target board or the tool requires a two row male connector with pin to pin spacing of 1.27mm/0.050" x 1.27mm/0.050" and 0.016" square post width. A shrouded connector with center polarization is recommended.

Placement:

We recommend placing for LA-2770 the even and for LA-3770 the odd numbered pins on the edge of the board (probe flex cable won't get twisted).

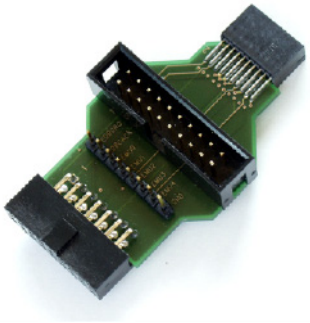
Example with housing: (surface mount)

MIPI-10: Samtec FTSH-105-01-L-DV-K
MIPI-20: Samtec FTSH-110-01-L-DV-K
MIPI-34: Samtec FTSH-117-01-L-DV-K

TI-20-Compact is a connector definition from Texas Instruments. The connector is smaller and carries more signals than the standard TI-14.

It has five EMU signals and supports RESET- and TDIS. EMUx are signals from Texas Instruments processors for additional programmable debug features. LAUTERBACH debuggers only support EMU0, which is used for the same purpose as DBGRQ and DBGACK. TDIS “Target Disconnect” signal must be connected to GND on the target side. It can be used to detect if the probe cable is connected to a target board. When using the converter below, TDIS is connected to GND on the debugger side. It is not used for target detection.

This converter can also be used for the TI-14.



ARM-20 Connector
TI-14 Connector (see LA-7748)
Debug Signal Description

Pinout TI-20-Compact:

Signal	Pin	Pin	Signal
TMS|TMSC|SWDIO	1	2	TRST-
TDI	3	4	TDIS (GND)
VREF-DEBUG	5	-	N/C (KEY)
TDO|-|SWO	7	8	GND
RTCK	9	10	GND
TCK|TCKC|SWCLK	11	12	GND
EMU0	13	14	EMU1
RESET-	15	16	GND
EMU2	17	18	EMU3
EMU4	19	20	GND

Target Connector:

The target board requires a 20-pin, double-row (two rows of ten pins) male connector with pin-to-pin spacing of 2.54mm/0.100 inch x 1.27mm/0.050 inch. Pin 6 (KEY) of the converter's female connector is plugged to prevent improper connection. Therefore, remove the terminal on pin 6 of the target connector.

Example: Samtec FTR-110-01-G-D-06, FTR-110-01-L-D

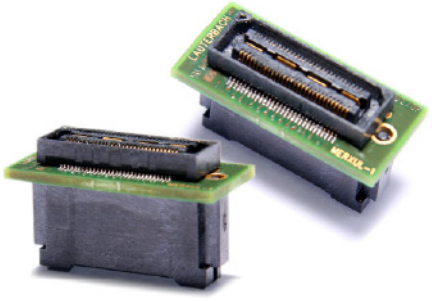
LA-3809 Converter Mictor-38/IDC20A to MIPI-20T

Converter for connecting an AutoFocus II Preprocessor and an IDC20A Debug Cable to a MIPI-20T connector. This allows you to use the AutoFocus II Preprocessor on the 4-bit wide trace port of a MIPI-20T connector.

ARM-20 Connector
Mictor-38 Connector
MIPI-20T Connector
Debug Signal Description
Parallel Trace Signal Description

LA-3817 Converter MIPI-60 to Mictor-38

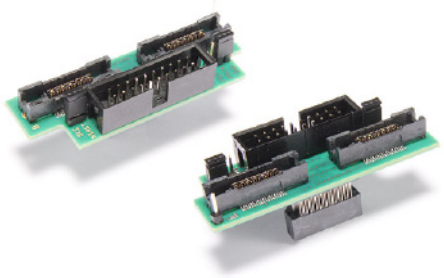
Converter to connect an AutoFocus II MIPI Preprocessor to a (single, <=16-bit) Mictor-38 connector on the target.



MIPI-60 Connector
Mictor-38 Connector
Debug Signal Description
Parallel Trace Signal Description

LA-3818 Converter 2xMictor38/IDC20A to MIPI-60

Converter to connect an AutoFocus II Preprocessor with one or two Mictor-38 ribbon cables and an IDC20A Debug Cable to a MIPI-60 connector on the target.



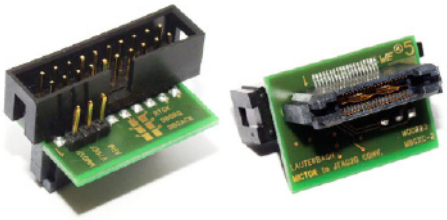
ARM-20 Connector
Mictor-38 Connector
MIPI-60 Connector
Debug Signal Description
Parallel Trace Signal Description

LA-3862 Converter IDC20A/MIPI-34 to Mictor-38

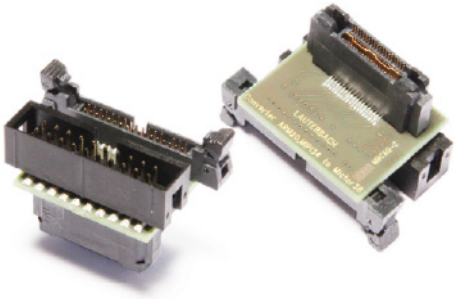
The LA-3862 and LA-3722 converters allow you to connect the IDC20A Debug Cable to a Mictor on the target.

If you have the AutoFocus II Preprocessor, you do not need a converter. You can connect the IDC20A Debug Cable directly to the Preprocessor, which routes the debug signals to the appropriate pins on the Mictor. However, if you have a LAUTERBACH tool for debug only and there is no separate connector for the debug signals on the target, then the LA-3722 is the recommended converter.

LA-3722:



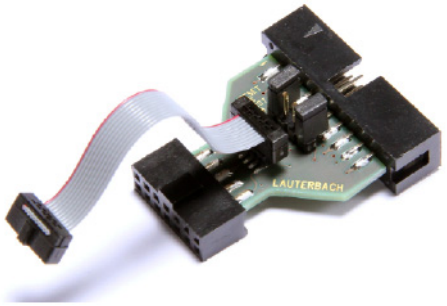
LA-3862:



ARM-20 Connector
Mictor-38 Connector
Debug Signal Description

LA-3863 Converter IDC20A to ALTERA-10/RISCV-10

Can be used to connect an IDC20A Debug Cable to an ALTERA-10 connector found on some Altera (Intel) evaluation boards.



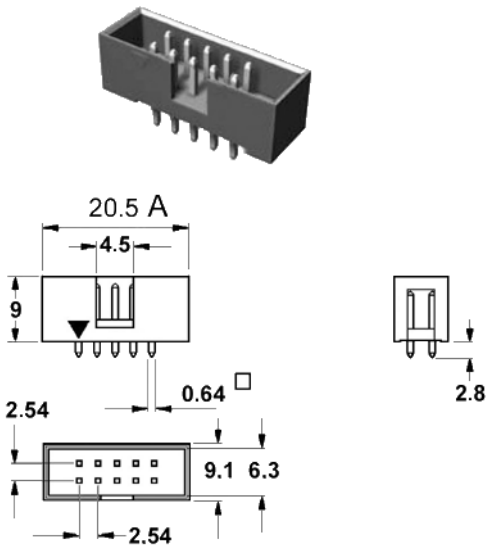
ARM-20 Connector
Debug Signal Description

Pinout ALTERA-10:

Signal	Pin	Pin	Signal
TCK|TCKC|SWCLK	1	2	GND
TDO|-|SWO	3	4	VREF-DEBUG
TMS|TMSC|SWDIO	5	6	[RESET-]
N/C	7	8	[TRST-]
TDI	9	10	GND

Pin 6 and pin 8 are optional and can be selected/deselected by jumper.

Target Connector 2.54mm:

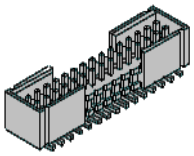


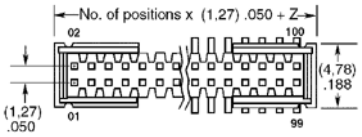
The target board requires a standard 10 pin double row male connector, pin to pin spacing 2.54mm/0.100" x 2.54mm/0.100" and 0.025" square post width. A shrouded connector with center polarization is recommended.

Examples with housing: Samtec HTST-105-01-L-D (through-hole), Samtec HTST-105-01-L-DV (surface mount)

Examples without housing: Samtec TSW-105-23-L-D, Berg: 67996-110H

Target Connector 1.27mm (Half Size):



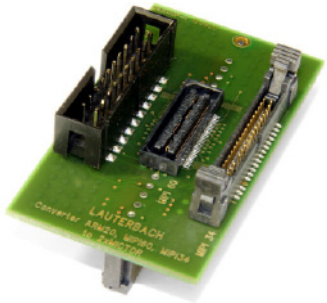


The target board requires a 10 pin double row male connector with 1.27mm/0.050" x 1.27mm/0.050" pin to pin spacing and 0.016" square post width. A shrouded connector with center polarization is recommended.

Example with housing: Samtec FTSH-105-01-L-DV-K (surface mount)

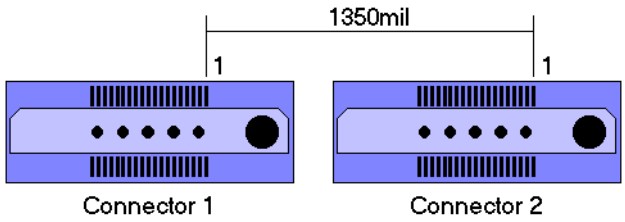
LA-3880 Conv. ICD20A, MIPI-34, MIPI-60 to 2xMictor-38

Converter for connecting an AutoFocus II MIPI Preprocessor and an IDC20A Debug Cable to (one or two) Mictor-38 connectors on the target. You may need to purchase one or two additional LA-1370 Mictor Flex Extensions if the Mictors on the target are not positioned exactly as they are on the converter.



ARM-20 Connector
MIPI-60 Connector
Mictor-38 Connector
Debug Signal Description
Parallel Trace Signal Description

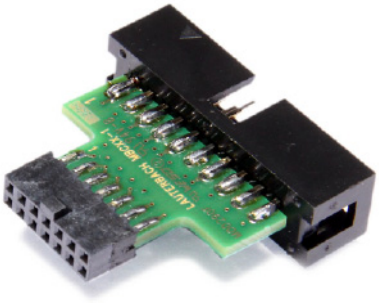
Placement:



A separation distance of 1350 mils is required for adaptation without flex cable or for optimum routing of the flex cables.

LA-3881 Converter IDC20A to XILINX-14

It can be used to connect an ARM-20 debug cable to a Xilinx-14 connector found on some Xilinx (AMD) evaluation boards.

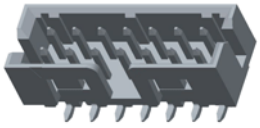


ARM-20 Connector
Debug Signal Description

Pinout XILINX-14:

Signal	Pin	Pin	Signal
GND	1	2	VREF-DEBUG
GND	3	4	TMS|TMSC|SWDIO
GND	5	6	TCK|TCKC|SWCLK
GND	7	8	TDO|-|SWO
GND	9	10	TDI
GND	11	12	N/C
GND	13	14	N/C

Target Connector:



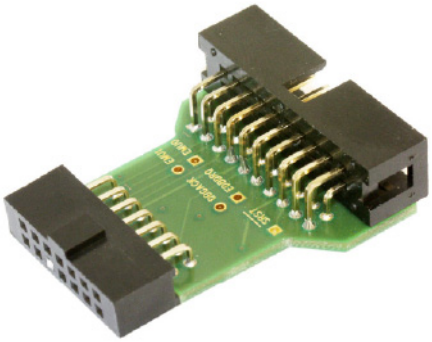
This is a 14 pin double row (two rows of seven pins) connector (pin to pin pitch: 2.00mm).

Example: Molex 87832-1420

LA-7748 Converter IDC20A to TI-14

This connector is defined by Texas Instruments and is used on many Texas Instruments target boards.

The TI-14 connector does not provide the RESET- signal and has EMU0 and EMU1 instead of DBGRQ and DBGACK. EMUx are signals from Texas Instruments processors for additional programmable debug features. The LAUTERBACH debugger supports only EMU0, which is used for the same purpose as DBGRQ and DBGACK.

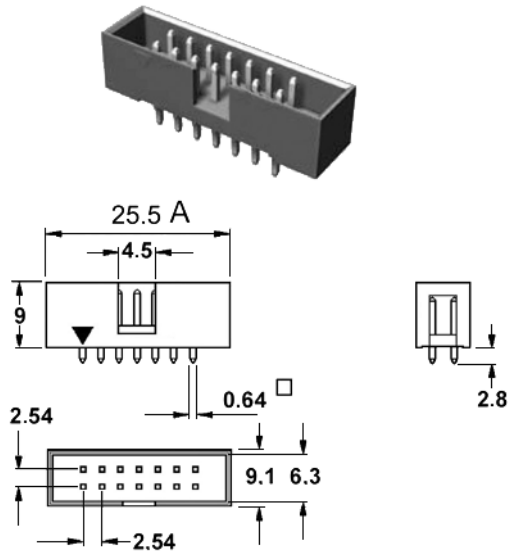


ARM-20 Connector
Debug Signal Description

Pinout TI-14:

Signal	Pin	Pin	Signal
TMS|TMSC|SWDIO	1	2	TRST-
TDI	3	4	GND
VREF-DEBUG	5	-	GND (KEY)
TDO|-|SWO	7	8	GND
RTCK	9	10	GND
TCK|TCKC|SWCLK	11	12	GND
EMU0	13	14	EMU1

Target Connector:



The target board requires a standard 14 pin double row male connector, pin to pin spacing 2.54mm/0.100" x 2.54mm/0.100" and 0.025" square post width. A shrouded connector with center polarization is recommended. Pin 6 of the converter's female connector is plugged to prevent incorrect connection. Therefore, remove the terminal from pin 6 of the target connector. If a terminal block without a cover is used, the space marked “A” must be a minimum of 23mm/0.9”.

Examples with housing: Samtec HTST-107-01-L-D (through-hole), Samtec HTST-107-01-L-DV (surface mount)

Examples without housing: Samtec TSW-107-23-L-D, Berg: 67996-114H