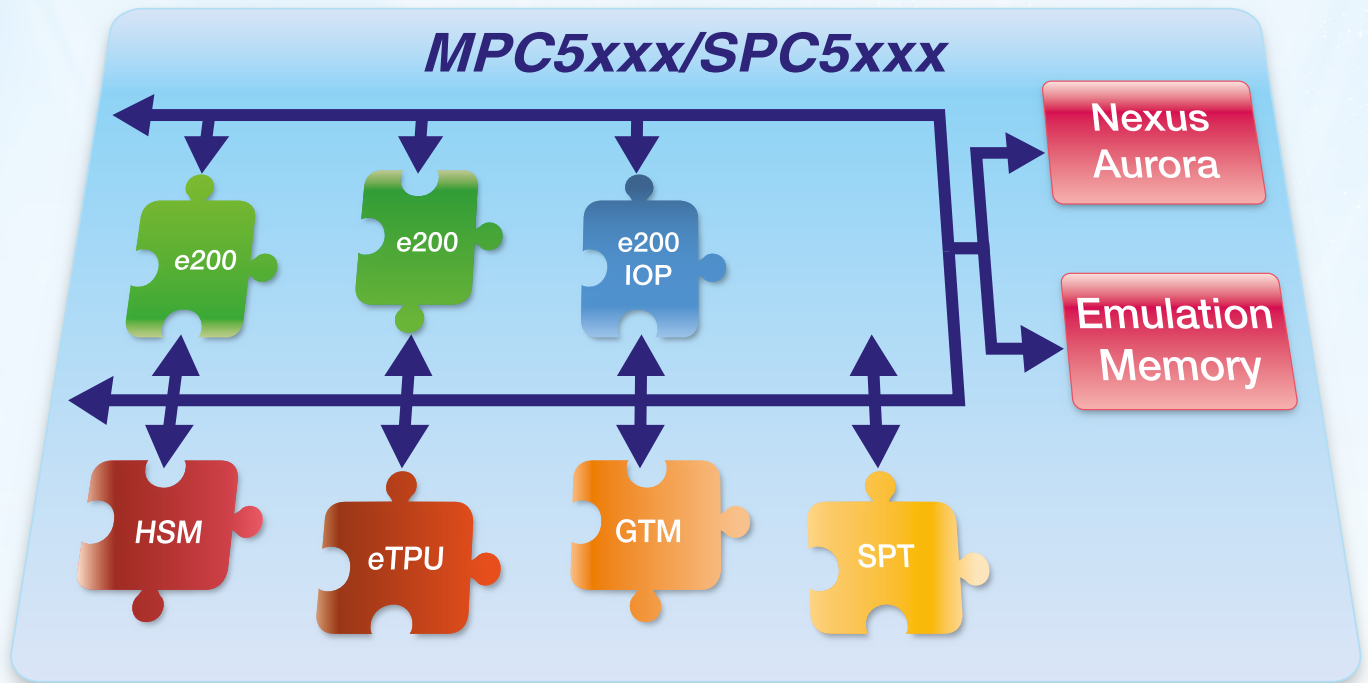


TRACE32®



Debug & Trace

NXP Qorivva MPC5xxx
STMicroelectronics SPC5xxx



MPC5xxx/SPC5xxx at a glance

For more than 10 years Lauterbach has supported the latest MPC5xxx/SPC5xxx microcontroller families. Our tool-chain offers:

- AMP and SMP debugging for e200, eTPU, GTM and SPT cores
- Multicore tracing via parallel Nexus, high-speed serial Aurora Nexus
- Multicore tracing to on-chip trace buffer (trace-to-memory)
- Trace support for peripheral modules (DMA, FlexRay, ETH, USB, ZipWire, ...)

Debugging the e200 Cores

The debug system TRACE32 for MPC5xxx/SPC5xxx provides high-speed access to the target processor via the JTAG/OnCE interface. Debugging features range from simple Step/Go/Break up to Autosar-OS aware debugging.

Customers value the flash programming performance of up to 450 KB/s and the intuitive access to all peripheral modules.

Debugging of complex chips		
target system	core type	core state
1: MPC5777M		
2: Core	PowerPC	running
3: Core	PowerPC	stopped
5: SMP Sub System	GTM	
0: Core	GTM	stopped
1: Core	GTM	stopped
2: Core	GTM	stopped
3: Core	GTM	stopped
4: Core	GTM	stopped
5: Core	GTM	stopped
6: Core	GTM	stopped
7: Core	GTM	stopped

Run	CPU	Misc	Trace	Perf
▶	Step			F2
▶	Step Over Call			F3
▶	Step Diverge Path			F4
↓	Go Next			
↶	Go Return			F5
↶	Go Up			F6
⏏	Go Till...			
▶	Go			F7
⏏	Break			F8
⏏	Mode			F9

TRACE32 offers the option to work in a debug environment including all e200 cores as well as all auxiliary controllers. You can inspect in detail the interaction between all cores and controllers.

TRACE32 allows concurrent debugging of all e200 cores.

- The cores can be started and stopped synchronously.
- The state of all cores can be displayed side by side.
- All cores can be controlled by a single script.

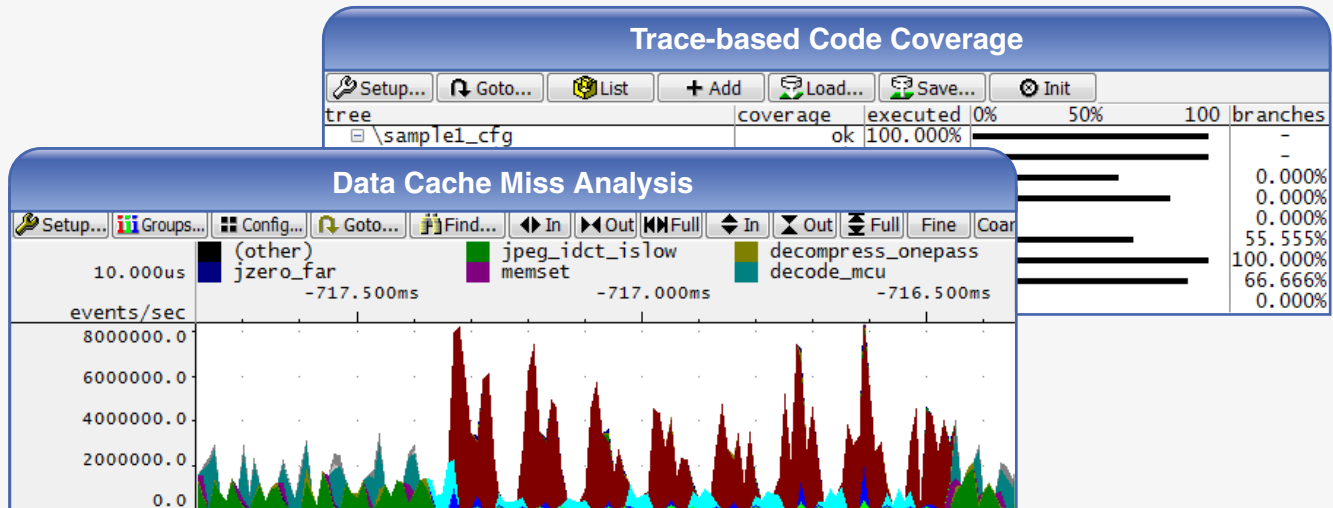
Multicore Debugging

Nexus Trace Solutions for MPC5xxx/SPC5xxx

Almost all MPC5xxx/SPC5xxx processors include a Nexus trace module, which enables tracing of program flow and data transactions. Depending on the processor, the Nexus module can route the trace data to one or more of the following destinations:

- An on-chip trace buffer with up to 32KB of trace memory (up to 2MB on emulation devices): This method is ideal to track down errors and in-field testing.
- A low/mid bandwidth off-chip parallel Nexus port for program flow and OS-aware tracing.
- A high bandwidth off-chip Aurora Nexus port for multicore and extensive data tracing.

The off-chip trace solutions can store up to 4GB of trace data and also provide the ability to stream the data to the host for long-term tracing, thus enabling effortless performance profiling and qualification (e.g. code coverage).



Support for Auxiliary Cores

Debugging and tracing of auxiliary cores is included free of charge:

- eTPU Timer Processing Unit – includes C-level debugging
- GTM Peripheral Timer Module
- SPT Signal Processing Toolbox

The screenshot shows the "eTPU Debugging" interface. It includes a toolbar with buttons for Step, Over, Diverge, Return, Up, Go, Break, and Mode. Below the toolbar is a table with columns for "addr/line", "code", "label", and "mnemonic". The code is for a function named "void CamDetect(unsigned char CamEdge, unsigned char CamStatus)". The table shows assembly instructions and their corresponding memory addresses, such as "P:000001DF BDFDB80" and "P:000001E0 4FFFFFF9".

The screenshot shows the "GTM Tracing" interface. It includes a toolbar with buttons for Setup, Goto, Find, Chart, Profile, MIPS, More, and Less. Below the toolbar is a table with columns for "record", "run", "address", "cycle", and "data". The table shows a list of records, including "ARU:0000007A data 16000ED816000898" and "D:00000124 wr-data 00000394".

Debugger and Trace for MPC5xxx/SPC5xxx

Power Debug

Debugger for Qorivva MPC5xxx

Debug cable with AUT026 connector supporting watchdog control, event signals and third-party tool handshake. Adapter to 14-pin OnCE header included.



Trace
License



On-chip Trace

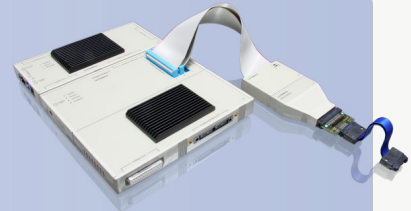
For devices with trace-to-memory feature: An additional license enables on-chip tracing support.

Power Debug

Power Trace

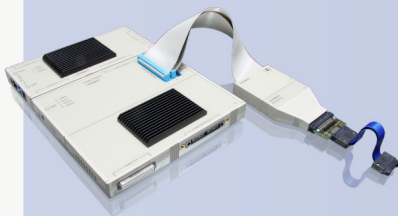
Parallel Nexus Trace

Trace port data rate up to 100 MHz DDR, enabled through AutoFocus technology.



Aurora NEXUS Trace

Up to 4 lanes with max. 6.25 GBit/s per lane
Reference clock up to 3.125 GHz

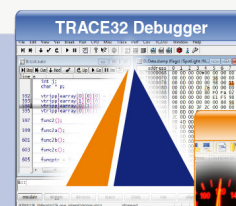


Power Trace

Front- End

Debugger for Synopsys Virtualizer

It allows debugging software designs before the first hardware prototype is available.



For more information visit: www.lauterbach.com/5500